FONIX®

FP40/FP40-D

(serial numbers 940000 and above)

MAINTENANCE MANUAL

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FRYE

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TABLE OF CONTENTS

1: INTRODUCTION

1.1 The FP40 Series 94

The FP40 Series 94 is an upgrade to the original FP40. It can be distinguished from earlier units by a serial number which is 94000 or above. The Series 94 uses a new CPU/SOURCE board which can, optionally, be configured to drive a color VGA monitor. This manual only includes information pertaining to the series 94 FP40. For older units, use the Maintenance Manual for FP40 serial numbers 0001-4999.

The series 94 CPU/SOURCE BOARD uses a newer generation processor. It also has an interface for a display daughter board. The Standard display daughter board will only drive the internal LCD. An optional VGA display daughter board is available that can drive a color VGA monitor as well as the internal LCD. The external speaker jack on the series 94 CPU is changed to a 3 conductor jack with a 3 mm instead of 1/8" diameter. The program EPROM is not interchangeable between the original and series 94 CPUs.

The DIGITIZER BOARD has changes to remove noise generated by the new CPU. One of these modifications is an inductor which is added to the internal microphone cable.

The LCD INTERFACE BOARD has a different physical configuration.

The following boards have not been changed: The POWER SUPPLY BOARD, OFF-LINE SWITCHER BOARD, Backlight Inverter, and the LCD DISPLAY BOARD.

1.2 The FP40-D

The FP40-D is a desktop version of the FP40. It can be distinguished from regular FP40s by the thousands place digit in the serial number being 4000 or above. Portable operation using an internal 12V battery is not possible since some parts related to that option are left off the POWER SUPPLY BOARD. The Operate button is left off the KEYBOARD and so the mains switch must be used to turn the instrument on and off.

2. SPECIFICATIONS

SINE SIGNAL

Frequencies Normal Sweep	1/12 octave frequencies from 200 to 8000 Hz, closest 100 Hz, within 1 %: 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.4, 2.5, 2.6, 2.8, 3.0, 3.1, 3.3, 3.5, 3.7, 4.0, 4.2, 4.5, 4.7, 5.0, 5.3, 5.6, 6.0, 6.3, 6.7, 7.1, 7.5, 8.0 kHz
Frequencies Fast Sweep	0.2, 0.3, 0.4, 0.5, 0.6, 0.8, 1.0, 1.2, 1.6, 2.0, 2.5, 3.1, 4.0, 5.0, 6.3, 8.0 kHz
Frequencies Short Sweep	0.2, 0.5, 0.7, 1.0, 1.5, 2.0, 3.0, 4.0, 6.0, 8.0 kHz
Warbled Sinewave	Has a 5%, 33-1/3 Hz warble
Amplitude (RMS)	Coupler mode: 40 dB SPL through 100 dB SPL in 5-dB steps. Probe mode: 40 dB SPL through 90 dB. Accuracy at reference point, after leveling, 2.5 dB for 500 Hz through 3500 Hz; 3.5 dB for all other frequencies.
Harmonic Distortion	(at 70 dB SPL) Less than 0.5% for 500, 800, and 1600 Hz

COMPOSITE SIGNAL (optional)

Frequencies	From 200 Hz to 8000 Hz in 100 Hz intervals. Accuracy within 1%
Amplitude	Coupler mode: (RMS) 40 dB SPL through 100 dB SPL in 5-dB steps. Probe mode: 40 dB SPL through 90 dB. Accuracy at reference point, after leveling, 2.5 dB for 0.5 kHz through 3.5 kHz; 3.5 dB for all other frequencies
Crest Factor	Less than 9 dB

BATTERY CURRENT MEASUREMENT

Measurement Range	0 mA to 25.5 mA
Current Limit	0 mA to 55 mA
Accuracy	3% of full scale ± 1 digit

Resolution	0.1 mA
Simulated Battery Types	5, 10 A/230, 13, 312, and 675 zinc air; 13, 312, 675, and 41 mercury; 13, 312, and 76 silver; AA
Battery Voltages Supplied	1.5 V for silver oxide and AA, 1.3 V for mercury and zinc air
Tolerance	± 0.01V, no load
Battery Type Selection	Under software control from front panel, but proper size battery pill must be selected

DIGITAL READOUT OF SPL

Frequency Range	200 Hz through 8000 Hz
Amplitude Range	0 dB SPL through 149.9 dB SPL –70 dB through +100 dB gain
Max Input Signal	150 dB SPL
Resolution	0.1 dB
Type	True RMS in composite mode
	True RMS in puretone if source >=90 dB in coupler mode, or >=85 dB in probe mode, filtered fundamental at lower levels
Accuracy	From 250 Hz to 2500 Hz, 2 dB ± one digit. All other frequencies, 3 dB ± one digit

SYSTEM NOISE

Equivalent Input Noise	50 dB SPL RMS
Crosstalk, Probe to Ref Mic	200 Hz: 76 dB below probe signal 8000 Hz: 80 dB below probe signal
Crosstalk, Ref Mic to Probe	200 Hz: 73 dB below reference mic signal 8000 Hz: 73 dB below reference mic signal
Noise Reduction	Averages the measured signal in synchronism with the signal generator by the factor chosen. Averaging factors from 2 to 16 available in powers of 2. Random noise will be reduced by an amount equal to the inverse square root of the factor chosen.

HARMONIC DISTORTION ANALYSIS

Type	2nd, 3rd, and 2nd + 3rd = total
Resolution	0.1%
Reading	Percent with respect to total signal. Readings made at frequencies from 400 through 2500 Hz

POWER REQUIREMENTS

Voltage	90 VAC to 264 VAC
Frequency	50 Hz to 60 Hz
Power Dissipation	40 VA at 120 VAC, 60 Hz input, normal operation

BATTERY OPERATION (optional)

Remote Operation	Requires optional battery power module. Operation possible for 3 hours continuously on battery power (with new battery at 25°C).
Auto Shutdown	General shutdown after no operation of controls for 15 minutes (battery operation only)
Battery Charger	Built-in automatic battery charger. Full charge in 10 hours.

DISPLAY

Liquid Crystal Display	Graphical display, 640 pixels wide x 200 pixels high
Color	Blue background with white lettering or white background with blue lettering
Illumination	Fluorescent edge lighted
Display Angle	Module tilts from 12° to 90° with respect to horizontal
Optional VGA Monitor	External
Resolution	640 x 480 color pixels

PRINTER

Internal Type	High speed, thermal
Print Speed	Screen copy in 14–19 seconds

Paper Used	Black print on white background. Print density adjustable in software for FP40 only.
Paper Width	60 mm
Access	Through top mounted door
External Printer	Signals are available at the rear panel RS232 connector to drive customer-provided printer with a serial input conforming to HPCL (monochrome or color) and Epson (monochrome or color) laser printer data format.

SOUND CHAMBER

Test Area	3" x 3" (7.5 x 7.5 cm) in acoustical foam-treated area. Separate space for excess microphone cord storage.
Loudspeaker	3" cone, mounted in case. Case mounts on a swivel arm for probe operation.

EXTERNAL CONTROLS, INDICATORS AND CONNECTORS

Front Panel Buttons	9 function keys plus Print, Feed, Data/Graph, Level, Reset, Start/Stop, and Operate On/Off (with guard ring)
Rotary Controls	Front: Amplitude, Frequency; Rear: Probe Monitor Level
A/C Power Switch	Rocker type, rear mounted
LEDs	Line Power : (Green LED indicates AC mains connected and rear panel External Power switch is ON.) Operate: (Green LED indicates that the FP40 is running from either internal battery or AC mains.)
Jacks	RS232 (9-pin), probe monitor earphone (1/4" stereo), external speaker jack (3.5 mm stereo phone), 15-pin VGA CRT connector

Line Power Connector	IEC320 (computer type)

PHYSICAL DESCRIPTION

Dimensions	20.125" x 14.750" x 6.5" (50.5 x 36.9 x 16.25 cm) (with lid on case)
Color	Light grey with black trim, white control panel
Weight	**FP40**: 25 pounds (11.4 kg) with lid and battery; 22 pounds (10 kg) without battery **FP40-D**: 16.5 pounds without accessories

OPERATING/STORAGE CONDITIONS

Altitude	Operating: 0 to 7500 feet (0 to 2286 meters) Storage: 0 to 50000 feet (0 to 15240 meters)
Humidity	Operating: 5 to 90% relative humidity (non-condensing) Storage: 5 to 90% relative humidity (non-condensing)
Temperature	Operating: 15–35° Celsius (59–95° Fahrenheit) Storage: 0–70° Celsius (32–158° Fahrenheit)

3. SPECIFICATION TEST PROCEDURE

3.1 Frequency Accuracy

Instrument required: Frequency counter accurate to 0.1 percent and capable of measuring 1000 HZ

Put the FP40 in puretone mode and enter the Coupler main screen. Set the amplitude to 100 dB SPL and the frequency to 1000 Hz. Connect the frequency counter to the External Speaker Output Jack.

The Frequency Counter should read 1000 Hz within the tolerance of the Counter plus the specified tolerance of the FP40.

3.2 Frequency Response

Instrument required: Precision sound level meter with 1/2 inch condenser microphone, response set to flat frequency response

Put the FP40 in puretone mode and enter the Coupler main screen. Be sure that Noise Reduction in the FP40 is turned off. Place the precision sound level meter microphone at the reference point in the sound chamber. Place the FP40 Coupler microphone so that its grill is facing the sound level meter's grill and within 1/8" of it. Set the FP40 level to 90 dB SPL.

Starting at 200 Hz, measure the RMS levels at the reference point with both systems for each puretone frequency. They should agree within the tolerance of the sound level meter plus the tolerance of the FP40.

3.3 Sound Level at Reference Point

Use the same setup as called for in 3.2 for measuring frequency response. LEVEL the FP40.

Starting at 200 Hz, measure the RMS level at the reference point with the sound level meter for each puretone frequency. It should read 90 dB SPL within the tolerance of the sound level meter plus the tolerance of the FP40.

3.4 Attenuator and Scaling Accuracy

Equipment required: Precision AC. voltmeter

Put the FP40 in puretone mode and enter the Coupler main screen. Be sure that Noise Reduction in the FP40 is turned off.

Set the frequency to 1 kHz. Patch the electrical drive signal from the External Speaker output jack back into the microphone input jack and also into the input of the precision AC voltmeter.

Note the input level in dB SPL, the measured voltage and the output level in dB SPL. Change the level in 10 dB increments and note that the levels all change by 10 dB. Make sure that the readings on the measuring voltmeter are within the tolerance of the sound level meter plus the tolerance of the FP40.

Caution: Make sure that an adequate signal to noise ratio is maintained. This can be important in getting good measurements, especially at low signal levels.

An attenuator may be needed to reach the lower levels on the Digitizer. This may be formed by use of a series resistor and a shunt resistor of 1000 Ω across the microphone input. A high resistance drive to the microphone input should be avoided because of shunt capacitance that is added to this circuit for purposes of RF interference rejection.

3.5 Battery Current Measurement

Equipment required: Precision D.C. voltmeter
Precision 1.5 kΩ resistor
Precision 100 Ω resistor

Make sure the Battery Simulator is turned on and enter the Coupler main screen. Remove any load on the Battery Simulator output and connect the voltmeter to it.

Voltage accuracy:
Measure the voltage output and see that it is 1.5 volts while in the silver positions and 1.3 volts while in the mercury and zinc air positions, within the voltmeter's accuracy plus the FP40's specified tolerance.

Current measurement accuracy:
Connect the 1.5 kΩ resistor to the output terminals of the Battery Simulator. Set the Battery Simulator to silver type 76. Read the battery current on the FP40 display. See that the reading is 1 mA within the tolerance of the above measured voltage,

the tolerance of the 1.5 kΩ resistor, the tolerance of the voltmeter, plus the specified tolerance of the FP40. Replace the 1.5 kΩ resistor with the 100 Ω resistor. Repeat the above test. The new reading should be 14.3 mA within the above tolerance.

4. CIRCUIT DESCRIPTION

4.1 System Overview

The FP40 is a hearing aid analyzer. It can test hearing aid frequency response in puretone (one frequency at a time) or, optionally, composite (79 frequencies all at once). Two input channels are available: reference and, optionally, probe.

The FP40 contains 8 (or optionally 9) circuit boards:

•KEYBOARD
•CPU/SOURCE BOARD
•STANDARD OR VGA DISPLAY DAUGHTERBOARDS
•LCD INTERFACE BOARD
•BACKLIGHT INVERTER
•DIGITIZER BOARD
•EQ BOARD (with probe option)
•POWER SUPPLY BOARD
•OFF-LINE SWITCHER

One crystal is used to synchronize everything except the off-line switcher and the LCD backlight inverter. Power supply ripple is synchronous with signal measurements and therefore does not affect the measurements.

The FP40 is capable of operation from AC mains anywhere in the world or, optionally, battery operation. Battery operation requires special software.

This unit has a hearing aid battery simulator, backlit LCD, fast hot dot graphics printer, and integral sound chamber.

The FP40 uses a serial bus to communicate with the POWER SUPPLY BOARD and the DIGITIZER BOARD. The serial bus carries printer data, printer control, power status, digitizer control, A/D, and battery simulator control. The serial bus has an addressing mechanism. The address determines whether a read or write operation is taking place.

The CPU/SOURCE BOARD is highly integrated. It includes the CPU, a clocked serial bus interface to communicate with the other boards, a dual RS232 interface, keyboard interface, display interface, and the sound source.

4.2 Mains Connection

The FP40 has two user replaceable primary fuses. The fuses protect against faults in the off-line switching power supply. The fuse normally located on the off-line switcher has been replaced with a shorting bar.

Since the off-line switcher built in input filter has excessive safety earth leakage current, it has been disabled by isolating it from chassis ground; note the plastic standoffs on the primary side mounting holes. A separate, low leakage, medical grade input filter is provided.

4.3 Off-Line Switcher

The off-line switcher is located under the printer mechanism. It converts any mains voltage in the world to +15.75 volts / 2.5 amps. The off-line switcher will slowly overheat if operated without a load. A 4 watt minimum load will prevent overheating.

4.4 Power Supply Board

Refer to Schematic for POWER SUPPLY 061-0106-XX
(3 pages, including printer driver)

4.4.1 AVAILPWR

AVAILPWR is the highest voltage available (less a diode drop) from the battery or 15.75 volts from the off-line switcher. It is created at the junction of D6 and D7.

4.4.2 On-Off Register

4.4.3 Turn On (FP40 only)

Signal POWERTOG originates at the front panel OPERATE push button. POWERTOG passes through the CPU/SOURCE BOARD and is sampled by CPU/SOURCE U6 pin 4. It then goes to power supply Q4.

The front panel OPERATE switch pulls POWERTOG from AVAILPWR to ground. As C12 charges it turns on Q4. U2 Gets Vcc power and generates +5REF. SYS RES\ forcing RS flip flop U15 pin 8 high. U15D pin 11 is still low. Q5 conducts about 1 mA and holds Q4 conducting after C12 charges.

4.4.4 Operator Turn Off (FP40 only)

The normal process of turning off the FP40 is:

The operator presses OPERATE switch.
The CPU senses POWERTOG low on the CPU/SOURCE BOARD.
The CPU sends a 5 second warning.
The CPU toggles POWERDOWN\ which sets U15C, pin 8, low.
Q5 no longer conducts; the on-off register at Q4 is set to off.

4.4.5 Hardware Only Shutdown (FP40 only) (Operator Controlled)

If the CPU malfunctions, the FP40 can be turned off by holding the OPERATE switch down for about 5 seconds. C50 charges through R99. After the 5 second time interval, U15D pin 11 goes high, Q5 current goes to zero, and the on-off register at Q4 goes to the off state.

4.4.6 Hardware Only Shutdown (Undervoltage)

U2 will shut down the Power Supply if U2, Pin 7 falls below 8.2 volts.

4.4.7 Hardware Only Shutdown (Service Technician)

When servicing the FP40, remove jumper J9 to disable the power supplies.

4.4.8 25600 HZ\SYNC

The PWM regulator will free run at power up at about 21.45 kHz. Once the FP40 has reached normal DC operating voltages, the CPU generates 25600 HZ\. When triggered by the falling edge of 25600 HZ\, one shot U6A generates a 350 nSec positive pulse. The pulse is passed through R15 and D2 to C9. C9 is suddenly charged above the trip point of the oscillator in U2. U2 immediately discharges C9 and starts another timing cycle.

4.4.9 PWM Regulator

U2 has an undervoltage lock-out which must have 9.0 volts at pin 7 to start operating and 8.2 volts at pin 7 to continue. U2 Vcc current is about 11 mA. This causes about a 0.5V drop across R18. Add 0.7V for D6 and the hardware low battery shut down point is about 9.4 volts. The PWM regulator compares the voltage on C51 (+5.0 volts) against U2 internal reference and uses this comparison to vary a pulse width derived from the clock on U2 pin 4. The output, U2 pin 6, controls the DC to DC converter.

This type of PWM regulator can develop a low frequency parasitic oscillation, “squagging”, if the output is on more than 50% of the time. Q2 and Q3 form a “super alpha” low offset (for discreet transistors) fast amplifier. R14 and R13 divide the clock ramp at U2 pin 4 so that the ramp reaches 1.0V at 50% duty cycle. The “I SENSE” input of U2 has a threshold of 1 volt and will reset U2 at about 50% duty cycle.

4.4.10 DC to DC Converter

U2 pin 6 goes positive to voltage AVAILPWR and turns on Q1. The current I through T1 primary = PRIMARY VOLTS x TIME / L. Primary current can get as high as 25 amps. Primary inductance $L \approx 7\ \mu$Hy, decreasing with primary current. When U2 pin 6 switches low, energy $E \approx 0.5 \text{ x } L \text{ x } I^2$ is dumped into the filter capacitors at T1. The snubbers prevent voltage overstress to Q1 as Q1 turns off. T1 primary is not perfectly coupled to the output windings. The energy left in the leakage inductance is dissipated in the snubbers.

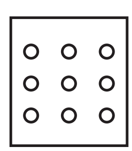
D14, a 5.6V zener connected between +5V and ground, will act as a crowbar and permanently short out if the PWM regulator goes out of control.

4.4.11 Current Limiter—Soft Start

If a power supply output is shorted, the energy stored in T1 will not be transfered to the filter capacitors before the next cycle begins. The primary current will begin increasing, not from zero, but from an already high value. If the voltage across 4 terminal resistor R52 exceeds 0.25 V, U1A and Q11 force U2 pin 3 positive. This will reset U2.

C5 causes the reference voltage at U1A pin 2 to build up slowly at power up. This causes the current limit to start low, then increase to 25 amps. This prevents a turn-on current inrush which could exceed the capability of the off-line switcher, which would then “brown out”. The undervoltage lock out on U2 would shut down the FP40 before it could power up.

MECCA



The central grounding point for the FP40, main MECCA, is located on the POWER SUPPLY BOARD. There are local MECCAs on other boards. Each local MECCA serves as central ground for that particular board. The local MECCAs only connect to chassis ground for the purpose of high frequency noise suppression.

4.4.12 Dummy Load

The dummy load provides a 4 watt (typical) load to the off-line switcher when the FP40 is not operating. Q13 and Q14 form a super alpha amplifier with small offset voltage. Power supply EXTPWR = 15.7V. R94 and R93 establish a 981 mV reference. If Q13 and Q14 are matched, R92 has 981 mV across it.

Q14 current = 272mA
R95 current = 9mA
R94 current = 5mA
Dummy current = 286 mA
Mains connected LED current = 10mA
Total standby power (no battery or battery charger)= 4.65 watts TYPICAL

4.4.13 Battery

Refer to FP40 Power Inputs Schematic

The main battery consists of two 6 volt, 3.4 amp x hour, sealed lead acid batteries wired in series. A 7.5 amp fuse provides protection from component failures in the FP40. The 22.1K resistor provides protection from component failures and accesses a test point for the FP40 A/D converter to measure battery voltage without effect of the voltage drop across the 7.5 amp fuse. The CPU continuously monitors battery voltage, and turns off the FP40 if battery voltage falls below about 10 volts. This prevents reverse polarizing any of the battery cells.

4.4.14 Battery Charger

U3, UC3906, is a sealed lead acid battery charger IC. U3 is wired to be a 2 state battery charger: bulk charge and float charge. Assuming a discharged battery, the FP40 is connected to AC mains. The battery charger is set to 14.8 volts with a current limit of 0.5 amps. The battery will begin with voltage less than 14.8 volts. The 0.5 amp limit will be in effect. The battery will charge to 14.8 volts. When the battery current falls to 50 milliamps, the battery charger switches to float charge; the charge voltage falls to 13.8 volts and prevents outgassing of hydrogen from the battery.

When the FP40 is printing, Q10 and Q12 disable the battery charger to provide more power to the printer.

4.4.15 Battery Voltage Buffer

Circuitry at U7A divides the battery voltage by 4. Signal “MAIN BAT VOLTS/4” is available to the A/D converter.

4.4.16 Status Port

The status port is a parallel input, serial output, tri-state, shift register. It reports battery charger status, printer status, and AC mains status to the CPU.

4.4.17 Printer Mechanism

The printer mechanism contains a unipolar stepper motor, a 320 dot thermal print head, print head thermistor, 2 paper out sensors, and a 320 element shift register. The shift register is loaded with a line of 320 dots to be printed by the FP40 serial bus. 5 segments of 64 dots are heated, one segment at a time, in order to minimize power supply current surges. Neither the printer mechanism nor the FP40 power supply could withstand all 5 segments burning simultaneously.

4.4.18 Burn Time One Shot

The burn time one shot U8 provides the print head with a 25 volt pulse to heat the dots in a segment to printing temperature. R40 and the parallel print mechanism thermistor provide thermal compensation for print density. U9 allows the duration of the pulse to be varied under CPU control.

PRINT DENSITY SETTING	U8 PIN 5 CONTROL VOLTAGE	U8 PIN 3 MIN uSEC	U8 PIN 3 MAX uSEC
0	1.224	147.5	196.3
1	1.575	204.8	258.6
2	1.927	268.0	328.0
3	2.278	338.5	406.3
4	2.630	418.3	496.1
5	2.982	510.0	601.5
6	3.333	618.0	728.8
7	3.685	749.3	890.0

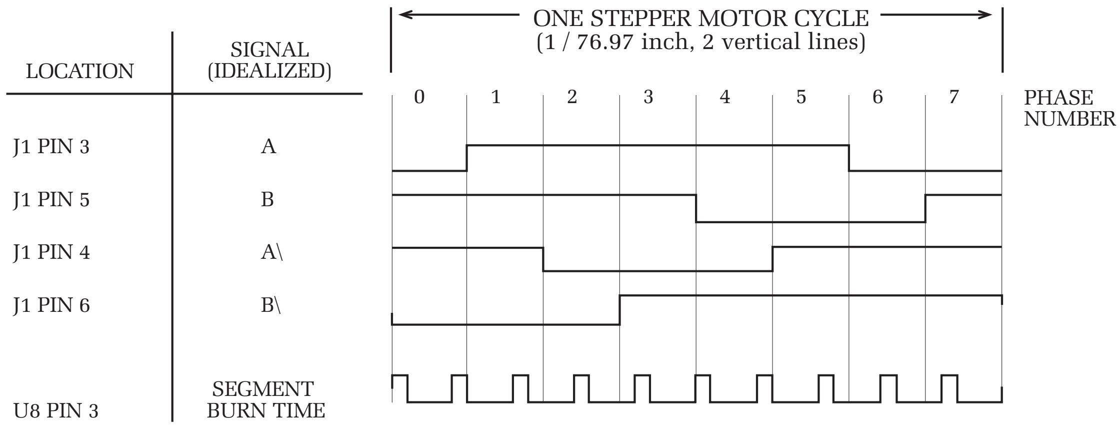
CALCULATION BASED ON THERMISTOR REPLACED WITH 10.0K RESISTOR.

U9 switch number is not to be confused with PRINT DENSITY SETTING. U9 hookup is optimized for minimum circuit board space.

The FP40-D print density setting is fixed at “5”.

4.4.19 Stepper Motor Driver

U16 is a SN75437 interface driver. The stepper motor is driven 12 volts instead of its rated 25 volts. Decoding of the stepper phases and burn triggering are done by the CPU. The FP40 applies “unipolar 1-2 phase magnetic excitation”.



There are 8 phases per stepper motor cycle,
4 phases per vertical line
153.94 lines per inch (both horizontal and vertical)
5 segment burns per vertical line
64 dots in each segment
320 dots total per vertical line

Inductive voltage spikes caused by the stepper motor are not shown.

4.5 Digitizer Board

Refer to Schematic for FP40 DIGITIZER BOARD 061-0102-XX (3 pages)

The DIGITIZER BOARD processes and converts electrical signals from the probe microphone and the reference microphone into 8 bit numbers. The DIGITIZER BOARD also contains the hearing aid battery simulator. The circuit reference numbers (R111, etc.) in this description apply to 061-0102-07, 061-0102-08, and 061-0102-09.

Reference numbers in brackets [ ] apply to the 061-0102-07 Digitizer when they differ from the -08 and -09. Earlier DIGITIZER BOARDS had a different set of circuit reference numbers.

4.5.1 Probe Mic Preamp

The probe microphone contains an electret condenser microphone element which is located at the end of an imperfect acoustic transmission line. J4 provides power to the probe microphone. The microphone element contains a JFET source follower. In the FP40, we exchanged the source and drain terminals of the microphone element in order to modify the operating mode. Source and drain terminals are reversible in normal JFETs. The new "source" terminal is connected to R111, 75K to -8V. This allows the output of the probe microphone to swing below ground. The dynamic range of the microphone is increased. J5 connects to the EQ board. The EQ board contains components matched to the probe microphone included with your FP40—two pre-emphasis networks and a lowpass filter.

The voltage at VR2 wiper is defined: 150.5 dB SPL = 5 volts peak to peak.

4.5.2 Headphone Amplifier

The headphone amplifier uses the probe microphone to allow the FP40 operator to listen to the client's hearing aid while the hearing aid is in the client's ear. R125 [121] and R127 [122] limit amplifier U28 power dissipation if the monitor headphones are shorted to chassis.

4.5.3 Reference Mic Preamplifier

The reference mic preamplifier provides a small amount of amplification to the reference microphone signal. The reference mic preamplifier output is defined: 150.5 dB SPL = 5 volts peak to peak.

4.5.4 Mic MUX

The CPU causes U18A to switch between reference microphone and probe microphone at a slow rate; less than 10 Hz. R60 [69] and R65 [63] protect U18A from overcurrent from U20 and U27B.

4.5.5 Rumble Filter

U22A forms a 56 Hz high pass filter with a Q of 0.5. This filter is used to remove low frequency ambient noise.

4.5.6 Prescaler

U22C, U22D, U25A, and U25B form the FP40 prescaler. The prescaler is a programmable gain amplifier chain. Control signals PREA...PREG control gain with a coded binary 1 dB step size over a 100 dB dynamic range. Logically PREG should have a value of 64 dB; however, only an additional 43 dB was required to meet the needs of the FP40. The control lines going to U29 and U24 are coded to allow close packing of the gain determining resistor chain. The 4051 IC pinout is not optimized for connection to chains of resistors. The gains in the various stages are staggered to keep the gain at each stage 22 dB or less.

4.5.7 SELFCAL

U15C allows signal CALSIG from the CPU/SOURCE BOARD to be applied to the anti-aliasing filter to allow the CPU to compensate for imperfections in the anti-aliasing filter. The anti-aliasing filter frequency response is flat enough so that this feature has not been implemented in software.

4.5.8 Anti-Aliasing Filter

The anti-aliasing filter removes frequencies above 17.6 kHz which could appear as frequencies 8000 Hz and below when measured by the A to D converter. These aliasing frequencies actually begin above the system Nyquist frequency 12,800 Hz (sample rate 25,600 Hz /2). Anti-aliasing filter operational parameters are listed on the schematic.

4.5.9 Speech Weighting Filter

U19A is a 900 Hz pre-emphasis network that complements the frequency response of the de-emphasis network on the CPU/SOURCE BOARD. R54 [53] prevents the gain from increasing without bound at high frequencies.

4.5.10 Level Clamp

R53 [51] and R38 [33] center audio signals to 1/2 scale (2.5V) for the A/D converter. CR1 and CR2 limit the input signal to the dynamic range of the A to D converter (0 to 5V).

4.5.11 Track and Hold/Multiplexer

The track and hold function is established at U10 pin 6 and U1A. The track and hold is kept exactly synchronous with the 25600 Hz reference frequency of the FP40. U1A pin 3 goes high when 25600 Hz is low (generating a CPU interrupt to start the A/D converter) or when the A/D converter is actually in use. This disables U10 pin 6. There is a guard run on both sides of the circuit board to protect U11A pin 3 from stray leakage currents when the circuit is in the HOLD mode.

The multiplexer can select the input audio signal, hearing aid simulator current, hearing aid simulator voltage, or FP40 main battery voltage.

4.5.12 Analog to Digital Converter

The A/D converter is an 8 bit serial output device in an 8 pin package. When U4 pin 1 “CHIP SELECT\” goes low, serial clock appears at U4 pin 7. Pin 6 “SOMI” will go from high impedance to “0”, then output 8 bits MSB first, with each serial clock negative edge, and then go back to a high impedance state when "CHIP SELECT\" returns to inactive high. Signal SOMI (slave out master in) is a 3 state line and is shared with other devices on the serial bus. R2 protects U4 in case of a fault on the serial bus.

4.5.13 Hearing Aid Battery Simulator

The hearing aid battery simulator has 4 elements:

- Voltage selector (U13) 0V, 1.0V, 1.3V, 1.5V
- Impedance selector (U17) 0Ω 2.4Ω 3.9Ω 4.9Ω 5.9Ω 7.9Ω 9.9Ω
- Voltage amplifier (U16 and Q1)
- Current amplifier (U14)

The voltage selector is straightforward. The 0V position allows the CPU to obtain a reading from the current amplifier when the current should be zero.

The voltage amplifier regulates the selected tap of the impedance selector to match the voltage selector output. Q1 drain circuit contains hearing aid current plus current from R48 [44]. The exact excess current = VSIM / R48 [44]. The excess current is subtracted from measured current to obtain hearing aid current.

The current amplifier is a crude instrumentation amplifier. R15 [25] is a current sense resistor. R15 [25] also limits current if the hearing aid simulated battery is shorted. R27 [23] causes the output of the current amplifier to be referred to +5REF. When the output current is zero, the output of the current amplifier will be +5REF.

4.5.14 Serial Bus Interface

For a serial bus transfer, U5 will contain the address. If the address is "11010000", then the contents of U12 and U26 will be updated. If the address is "0001000", then the A/D converter will be enabled.

4.5.15 Power Supplies

Most of the operational amplifiers on the DIGITIZER BOARD operate with ±8 volt power supplies. This allows the outputs to swing within the ±5 volt range of the CMOS 4051 and 4053 switches. The CMOS switches are not operated from +5V (digital) because noise on that supply would be coupled into signals passing through the CMOS switches.

4.6 Keyboard

Refer to Schematic for FP40 KEYBOARD 061-0103-XX

Because the KEYBOARD is difficult to service, only passive components are included on the board.

4.6.1 Key Switches

Each key switch consists of a silicon rubber actuator with attached conductive silicon rubber contact disk and 3 gold plated circuit board runs etched directly on the keyboard. Each key switch has a ground contact plus a pair of contacts for a unique pair of sense lines (2PST N.O.). The six available sense lines are: K1, K2, K3, K4, K5, K6.

The RESET key switch uses only one line separate from the 6 main sense lines.

4.6.2 Rotary Encoders

SW8 and SW9, "AMPLITUDE" and "FREQUENCY", are each 2 bit mechanical relative gray code encoders. As the encoder is rotated clockwise, the repeating gray code pattern for 1 - 2 - 3 - 4 is sent to the CPU. As the encoder is rotated counterclockwise, the repeating gray code pattern for 4 - 3 - 2 - 1 is sent to the CPU.

4.6.3 "Line Power" LED

This LED is lit when the FP40 is connected to AC power and the mains switch is turned on.

4.6.4 "Operate" LED (FP40 only)

This LED is lit when the FP40 main power supply is running.

4.6.5 "Operate" Keyswitch (FP40 only)

This is a mechanical plastic enclosed "dome" snap action switch, SPST N.O.

4.7 CPU/Source Board

Refer to Schematics for FP40 CPU-SOURCE BOARD 061-0131-XX (3 pages)

The CPU/SOURCE BOARD contains all CPU related functions, sound source, serial interface, keyboard interface, and display interface.

4.7.1 CPU

The 80C188EC is a 16 bit microprocessor with integrated peripherals. Inside U25 are:

- Oscillator circuit for crystal
- Enhanced 8088 Central Processing Unit (CPU)
- DMA controller #0 (used to output LCD refresh data)
- DMA controller #1 (used to output sound at 25,600 Hz rate)
- DMA controllers #2 & #3 are currently unused
- Asynchronous serial port #0 (for RS232 remote control)
- Asynchronous serial port #1 (for RS232 printer)
- Timer #0 (used by Standard Display board)
- Timer #1 (generates 25,600 Hz reference frequency)
- Timer #2 (used to time printer stepping states)
- Watch Dog timer (used to clock the Standard display board)
- Chip Select Unit (generates chip selects for memory & I/O)
- Interrupt Control Unit (accepts interrupts & routes to CPU)

Since the 80C188EC has a multiplexed address/data bus, U18 and U23 are needed to latch the address bus bits 0-7 and bits 16-19.

4.7.2 Clocked Serial Bus Interface and Addresses

The clocked serial bus interface is made up of: the SIO CONTROL\ line from U12, the SIMO output data line from U12, and the SOMI input data line going to U6.

The Serial port addresses are shown below:

"ADDRESS" SHIFT REGISTER BIT A B C D E F G H	IN/OUT (ref CPU)	DEVICE
0 0 0 1 0 0 0 0	IN	A/D CONVERTER
1 1 0 1 0 0 0 0	OUT	DIGITIZER CONTROL
1 0 1 1 0 0 0 0	OUT	POWER CONTROL
1 0 0 0 0 0 0 0	IN	POWER STATUS
1 0 0 1 1 0 0 0	OUT	PRINT HEAD
1 0 0 1 0 1 0 0	–	(SPARE)
1 0 0 1 0 0 1 0	–	(SPARE)
1 0 0 1 0 0 0 1	–	(SPARE)

Address shift registers on other boards receive data when signal SIO CONTROL is "1". When SIO CONTROL returns to "0", the outputs of the address shift registers are updated with the new address.

4.7.3 Memory Chip Selects

Chip select UCS\ on U25 selects the EPROM U17 and LCS\ on U25 selects the RAM U20. Each chip select is internally programmable. The EPROM is positioned at the top of address space and the RAM is positioned at the bottom.

Chip select GCS4\ is used by the VGA daughterboard to select its display memory.

4.7.4 Port Chip Selects

Chip selects GCS0\, GCS1\, GCS2\, GCS3\, and GCS5\ are used to select the I/O ports.

4.7.5 Output Parallel Ports

CHIP SELECTS	IC	FUNCTION
GCS0\		DISPLAY DAUGHTER BOARDS
GCS1\	U15	SOURCE DAC BUFFER
GCS2\	U19	SOURCE ATTENUATOR
GCS3\	U12	MISC OUTPUTS

4.7.6 Input Parallel Ports

CHIP SELECTS	IC	FUNCTION
GCS0\		VGA DAUGHTER BOARD
GCS3\	U6	PUSH BUTTONS
GCS5\	U7	ROTARY CNTRL & MISC

4.7.7 EEROM

U8 is a serial input/output 4K bit electrically erasable read only memory. It is organized as 512 bytes. The EEROM is used to store leveling curves and setup information even when the FP40 is turned off. Signal EECLK from U12 is used as a shift register clock in data transfers. The serial I/O data is routed by the EEDAT line directly to an I/O pin on U25.

4.7.8 Source DAC

U11 is a latched digital to analog converter. The CPU DMA transfers the next sound source word to U15 a short but variable time after the negative edge of signal 25600 Hz\. The opposite phase of the signal, 25600 Hz, is used to transfer the contents of U15 into U11 without any timing variations.

4.7.9 SELFCAL

"SELFCAL" causes U22A to switch a .528 V PK-PK signal to "CALSIG". This can be used by the CPU as a self test mechanism for the DIGITIZER BOARD. CALSIG is switched to ground when not in use to prevent crosstalk on the DIGITIZER BOARD.

4.7.10 Output Anti-Aliasing Filter

The output signal contains fundamental frequencies between 100 Hz and 8,000 Hz and is sampled at 25,600 Hz. Due to the sampling process, the DAC output also contains an infinite series of alias frequencies beginning at 17600 Hz (= 25600 - 8000). The output anti-aliasing filter removes these extra frequencies.

4.7.11 Attenuator

The output attenuator is formed by U22B, U24, and U26. It has 127 dB of dynamic range in 1 dB steps. The 74HC4051 control lines are coded to allow efficient physical placement of attenuator resistors. The 74HC4051 pinout is not optimized for attenuators.

4.7.12 Power Amplifier

U28 is a monolithic power amplifier with output short circuit protection and overtemperature shutdown. It is stable with gains of 10 or more. For stability, it is well bypassed by C56, C68, C66, and C65. CR14 provides electrostatic discharge protection. C73 and C74 provide radio frequency interference suppression and electrostatic discharge protection.

4.7.13 Display Area

The STANDARD DISPLAY DAUGTER BOARD plugs into J10. The VGA DISPLAY DAUGHTER BOARD plugs into J7 and J10. Either daughter board will continuously refresh for the LCD. The VGA board can also refresh a VGA monitor through connector J14.

The LCD INTERFACE BOARD plugs into J5.

U4 supplies the VEE (-20V) for the LCD. A resistor on the LCD INTERFACE BOARD sets this voltage for a particular LCD.

U5 determines the CONTRAST voltage for the LCD. The exact configuration of this opamp depends on the unique wiring and resistors on the LCD INTERFACE BOARD. Two inputs that affect CONTRAST voltage:

1) The setting of the front panel CONTRAST pot.

2) The temperature measuring diode inside the LCD assembly.

4.7.14 RS232 Ports

The dual asyncronous port in the 80C188EC, along with the interface chip U29, and connector J15, comprise the two RS232 ports. J15 is wired as a standard IBM PC 9-pin serial connector, except that the transmit and recieve lines for the second port use pins 4 and 6 instead of the DTR and DSR signals.

4.8 Standard Display Board 061-0132-XX

U1 and U3 accept each byte of display data from DMA0 on the CPU. These two chips also multiplex the two nibbles in each byte onto the LCD's 4 data lines.

U4B, U4A, U2B, and U5B make up the sequencer which controls the process of shifting the two nibbles into the LCD. The sequencer is clocked by the watch dog clock on the CPU.

U2A generates the AC drive signal for the LCD.

Timer 0 on the CPU is used to count the 160 nibbles on each line and generate the data latch signal (LP) when they are all shifted in.

4.9 VGA Display Board 061-0133-XX

U6 takes the 20MHz clock from the CPU and converts it into the two clocks needed by the VGA controller. U3 is the VGA controller. U1 and U5 are the DRAM display refresh memory. U4D and U2 are used to generate the memory and I/O read and write signals for the VGA controller. U4C, U4A and U4B are used to turn off the CRT display sync signals while in screen saver mode.

4.10 LCD Interface Board 061-0105-XX

The LCD INTERFACE BOARD contains unique wiring and resistors to allow connection to various manufacturers' LCDs without changing the FP40 CPU/SOURCE BOARD. All LCD signals pass through this board.

4.11 LCD Assembly

Refer to Schematic for LCD INTERFACE 061-0105-XX

LCD INPUT SIGNALS (pin 14 is an output)

LCD PIN #	NAME	FUNCTION
1	FLM	Beginning of frame
2	M	AC drive signal
3	CL1	Latches one horizontal line (160 nibbles)
4	CL2	Nibble clock; shifts 4 bits into LCD assy
5	DOFF\	DISP OFF\ ; “0” = display off
6	D0	Data bit; “1” = on
7	D1	Data bit; “1” = on
8	D2	Data bit; “1” = on
9	D3	Data bit; “1” = on
10	VDD	+5V
11	VSS	Gnd
12	VEE	-20V
13	Vo	Contrast voltage (user adjustable) ≈ -20V
14	ANODE	Anode, LCD temp sense diode; (cath = gnd)

4 bit nibbles are entered into the LCD beginning in the upper left hand corner, moving from left to right, then advancing one line at a time from top towards bottom.

LCD SCREEN

START [D3 D2 D1 D0] [D3 D2 D1 D0].............................
....
....
....
.... [D3 D2 D1 D0] END

4.12 Backlight Inverter Board

Refer to Schematic for LCD BACKLIGHT INVERTER – MODIFIED

IC1, uPC494, internal oscillator is disabled. The only function of IC1 is as a level translator. A logic level "0" on CN1 pin 3 passes through a string of inverters and turns on Q3. This supplies +12V to the saturated core oscillator at T1. The output of T1 supplies the fluorescent tube in the FP40 LCD.

5. SERVICE AND REPAIR GUIDE

5.1 Opening the FP40 for Service

When removing screws on the FP40, keep all lockwashers on the screws. Many lockwashers on the FP40 are required to insure that all chassis parts are connected electrically. This insures that the FP40 will operate in strong electromagnetic fields and insures product safety. In the event of a fault in parts connected to mains power, the chassis connection to power cord safety earth terminal must be solid (less than 0.1Ω).

To open the FP40 for service, remove the three screws and lockwashers on the vertical part of the rear panel. Open the sound chamber lid to prevent damage to the sound chamber lid foam. Lift the rear panel. The top section of the FP40 will pivot on a hinge at the front. Save the foam strip along the FP40 left side.

To gain access to parts on the POWER SUPPLY BOARD, remove the two screws and lockwashers on the rear panel horizontal lip. Lift this section and the DIGITIZER BOARD will pivot on a hinge along the front of the FP40.

Most cables inside the FP40 are identified with a color dot. The color dot indicates mating connector and orientation. If a cable is not connected correctly, serious damage may result.

Repair of the off-line switcher is not recommended. If the off-line switcher blows mains fuses, replace the off-line switcher. (See section 7 concerning the replacement of fuses.) Oscilloscope probing of primary circuits must be done only with a fully isolated AC supply connected to the off- line switcher mains input. Remember that the off-line switcher on board fuse has been transferred to the FP40 power input module. Hazardous voltages are present in the off-line switcher mains circuitry. Under certain fault conditions, lethal voltages may be present even after the off-line switcher has been disconnected from AC mains.

6. CLEANING

For your safety, disconnect the FP40 from mains power while cleaning.

Wipe the FP40 case with a slightly moist but not dripping cloth. Use plain water or water with mild dishwashing detergent. Wipe away any detergent with a slightly moist cloth, then dry the FP40.

Cleaning of the FP40 LCD screen should be kept to a minimum to avoid scratching the surface. To clean the LCD, first blow off any loose dust. Then wipe gently with a soft cloth moistened with glass cleaner. Starting in December of 1996, the surface of the LCD will be waxed to minimize scratching.

The microphones should be wiped with a dry cloth. Excess moisture may damage the microphone.

Never allow fluid to enter:

- the Liquid Crystal Display (LCD)
- the electronics module
- the power switch
- the power entry module
- the electrical connectors
- the keyboard push buttons or rotary controls

Solvents and abrasives will cause permanent damage to the FP40.

7. SAFETY MARKINGS

Right Side Panel Safety Markings:

CAUTION: FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH 250V, FAST 2 AMP FUSE

The FP40 uses two mains fuses of the same type regardless of the voltage used. Never replace a fuse with a fuse which has a rating higher than that shown.

The fuse must have at least one safety approval mark, either UL or CSA.

The fuse size is 1/4" x 1 1/4". Do not substitute 5 x 20 mm fuses. UL rated fuses will open at 1.4 times rated current; 5 x 20 fuses will open at 2.1 times rated current.

GROUNDING RELIABILITY CAN ONLY BE ACHIEVED WHEN THE EQUIPMENT IS CONNECTED TO AN EQUIVALENT RECEPTACLE MARKED HOSPITAL ONLY OR HOSPITAL GRADE.

Safe operation of the FP40 absolutely depends on the integrity of the safety earth connection at your mains outlet. If you have any doubts concerning the adequacy of your mains outlet, contact a qualified electrician.

Rear Panel Safety Warnings:

CAUTION
ELECTRICAL SHOCK HAZARD.
DO NOT REMOVE INSTRUMENT COVER.
REFER SERVICE TO QUALIFIED PERSONNEL.

12 Volt Battery Cover Safety Warnings:

FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH TYPE 3AG, STANDARD BLOW 7.5 AMP FUSE.

Never replace a fuse with a fuse which has a rating higher than that indicated.

The fuse must have at least one safety approval mark, either UL or CSA.

The fuse size 1/4" x 1 1/4" .

8. SCHEMATIC DRAWINGS

8.1 List of Schematics

Name	Part Number	Drawing Number
FP40 Block Diagram		999-2237-00
FP40 Power Inputs		999-2236-00
FP40 Off-line Switching Supply	116-0006-00	999-1738-00
FP40 Power Supply (1)	061-0100-08	999-1638-07
FP40 Power Supply (2)	"	999-1639-06
FP40 Power Supply (3)	"	999-1640-05
FP40 Power Supply (4)	"	999-2020-01
FP40-D Power Supply (1)	061-0100-18	999-2223-03
FP40-D Power Supply (2)	"	999-2222-02
FP40-D Power Supply (3)	"	999-2184-00
FP40-D Power Supply (4)	"	999-2185-01
FP40 CPU-Source (1)	061-0131-04	999-2217-04
FP40 CPU-Source (2)	"	999-2233-04
FP40 CPU-Source (3)	"	999-2234-04
FP40 CPU-Source (4)	"	999-1990-00
FP40 CPU-Source (5)	"	999-1991-00
FP40 CPU-Source (6)	"	999-1992-00
FP40 LCD Display	061-0132-03	999-2216-03
FP40 VGA Display (1)	061-0133-03	999-2215-04
FP40 VGA Display (2)	"	999-2021-00
FP40 LCD Interface	061-0105-01	999-1691-04
FP40 Digitizer (1)	061-0102-10	999-1561-12
FP40 Digitizer (2)	"	999-1562-12
FP40 Digitizer (3)	"	999-1563-12
FP40 Digitizer (4)	"	999-2023-00
FP40 Digitizer (5)	"	999-2024-00
FP40 Digitizer (6)	"	999-2025-00
FP40 Digitizer (7)	"	999-2026-00
Frye Mic EQ Board	061-0010-02	999-1324-03
Cable, Microphone Input, FP40 Model 94	119-0224-03	999-2237-00
FP40 Keyboard	061-0103-04	999-1573-03
FP40-D Keyboard	061-0103-14	999-2225-00
LCD Backlight Inverter - modified	061-1099-00	999-1719-00
'Y' Cable for Laser Printer Option		999-1793-01
FP40 Laser Connector	098-2869-01	999-1794-01
Laser Printer DB25P Connector	098-1870-01	999-1795-01
FP40 Battery Simulator Cable, mod history		999-1890-00
M200/M250 Microphones		999-2245-00
FM40 Microphone		999-2246-00
FP40 Telecoil Wand	043-1050-00	999-2644-00

Note: Raw circuit boards are marked with part number prefix "060-". The part number prefix changes to "061-" for assembled boards.