FONIX®
6500-CX

MAINTENANCE MANUAL

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MANUAL NOTE

The 6500-CX is the latest revision of the 6500 Hearing Aid Analyzer. The 6500-CX Maintenance Manual includes only schematics and descriptions pertaining to the 6500-CX. For servicing information pertaining to the 6500 and 6500-C (and older products partially upgraded to 6500-CX performance), also consult the 6500/6500-C Maintenance Manual.

Interchangeability (for upgrades from 6500 & 6500-C only):

New CPU boards and old CPU boards are interchangeable. Software to operate the two types of CPU differs. It will be necessary to identify the CPU board type when ordering software upgrades.

The new Fujitsu printer mechanism must be used with 061-0224-xx printer board. The old printer mechanism must be used with 061-0024-xx printer drive board.

The new Fujitsu printer mechanism plus 061-0224-xx pair is interchangeable with the slower older printer mechanism plus 061-0024-xx pair.

The two printer mechanisms require different widths of thermal paper:
The new Fujitsu printer mechanism requires 026-0009-00 paper.
The old printer mechanism requires 026-0011-01 paper.

Changes:

- The 6500-CX adds a faster, more powerful CPU; an auxiliary RS-232 interface option; a faster, high resolution printer; and optional safety certification.
- Front panel LEDs are changed to GREEN.
- Minor changes were made to chassis wiring.
- The power supply 5V regulator circuit was changed.

1. OVERVIEW

The 6500-CX, in its main mode of operation, produces a complete set of tones from 100 to 8000 Hz simultaneously, and is able to analyze the response of the hearing aid to this complex signal, displaying all of the 80 components simultaneously on a graphical CRT display, updating the display at the rate of twice a second. It also can operate in the pure tone analysis mode presently used in most hearing aid testing. The frequencies used are from 100 to 8000 Hz in 100 Hz increments. Sweep measurements do not include 100 Hz.

The composite technique has the immediate advantage that the response curve for the hearing aid can be viewed in “real time”, and for the first time the effects of altering the setting of a control can be viewed while it is being done. Another advantage of this technique is the capability of measuring the “real” response of an AGC hearing aid, instead of the artificially flattened one obtained with pure tone testing.

Analysis of the hearing aid output is done by first taking 256 samples of the signal. These samples are taken in exact synchronism with the signal generator.

These 256 samples are then passed through a mathematical process called the Fast Fourier Transform, which takes the timed samples and converts them into 128 frequency components. 79 of these components are then displayed on the CRT screen in the form of a graph.

A hard copy of the screen image is available through the use of the built-in thermal printer. The top half of the screen is printed first, followed by the bottom half, if required.

1.1 Signal Generation Overview

1.1.1 Digital Basis

The complex signal is generated by reading 256 12-bit data words in RAM sequentially and doing it over and over again. The program is able to adjust the individual amplitude of each signal component in the series so that it provides a correct amplitude of drive at the test point in the chamber for each test frequency. The test microphone is placed at the reference point in the chamber. Pushing the LEVEL button starts the amplitude correction process. A composite analysis of the chamber is done and correction factors are calculated which alter all of the individual drive components so that the chamber response is flat and at the desired amplitude at this reference point.

One way to think of the test waveform is to picture one sine wave of 100 Hz being built using 256 points or steps through the sequential reading of a 12-bit digital RAM. If we wanted to create a signal with two equal value components, we would arithmetically add to this wave a second sinewave, say of 400 Hz. Each cycle of the 400 Hz wave would take exactly one fourth as many steps as the 100 Hz wave to produce, or 64 steps. When these two sets of steps are added together we would get a composite wave with two frequency components.

1.1.2 Component Amplitude Weighting Considerations

The amplitude of each frequency may also be dependent upon its placement in the frequency spectrum. If a white noise equivalent is to be used, then every multiple of 100 Hz will be used and will have an equal value amplitude. If a speech spectrum is to be approximated, the amplitudes of the components in the spectrum will drop at a rate of 6 dB per octave above 900 Hz when viewed on a standard heterodyne or Fast Fourier analyzer. This sloped correction is produced by using analog filters, since we would very quickly run out of digital resolution while covering the 3 octaves between 900 and 7200 Hz. 18 dB equals a ratio of about 8 to 1.

After the signal is received from the hearing aid and passed through the preamplifier, it is run through a high frequency emphasis amplifier to restore the 6 dB/octave loss so that we can get a compensated gain response picture.

The RMS amplitude of the drive signal increases in proportion to the square root of the sum of the squares of all of its components. Thus, if a particular RMS value of drive signal is needed, both the number and the individual amplitudes of all of the components must be taken into account. A multiple frequency signal will then have smaller component amplitudes to produce the same RMS drive to the device under test as that of a sine wave signal drive which has only one frequency component.

1.1.3 Phase of the Components

Another interesting problem encountered is that the individual components of the wave cannot be allowed to line up in phase, or the composite signal will consist of a series of spikes with very little in between, or an impulse drive. The disadvantage with this type of drive is that it makes very heavy demands on the dynamic range of the hearing aid under test. Hearing aids are not known for their large dynamic ranges, so this type of waveform must be avoided. To produce a moderate crest factor noise equivalent, it is necessary to skew the phases of all of the components so that a given RMS amplitude of signal has a low peak value. A computer program was used to determine the optimum set of phase values.

1.1.4 Special Distortion Measurements

Harmonic distortion tests can be run by generating a signal consisting of only one sine component at a time, and using the Fast Fourier analysis program to determine the spectral distribution of harmonics.

Intermodulation tests are automatically run using the composite waveform. If present, this type of distortion is immediately apparent when viewing the gain or power response of the hearing aid.

1.2 Signal Detection Overview

1.2.1 Fast Fourier Technique

The assumed technique for making response measurements is the Fast Fourier Transform. This technique is ideally suited to a system that is used to analyze a digitally generated waveform, since the sampling process can be locked to the signal generation process, thus eliminating one of the main problems with the FFT, the windowing of the measured waveform. A rectangular window is thus possible and used. That is, all sampled components are used as measured.

1.2.1.1 Windowing

The FFT requires that the signal being sampled is exactly repetitive in order to achieve a clean spectral display. If there is an abrupt discontinuity between the first and last samples taken, the transform can only assume that large high frequency components are present in order to generate the discontinuity. Use of the internally generated signal helps to eliminate this problem; if a random noise is present in the signal being measured, it will appear in the response display.

When the sound drive is switched to “OFF” the 6500-CX is turned into a general purpose spectrum analyzer and can be used for analysis of signals. When this is done, mathematical windowing is used as is done with standard FFT analyzers. This windowing is done by multiplying the first and last samples taken by a value close to zero. The next two samples in from the ends are multiplied by a larger quantity. In the center of the group of samples, the values are multiplied by a compensating factor greater than unity. The windowing function used is called a Hanning function.

1.2.1.2 Aliasing

A further requirement is that the bandwidth of the measured signal be controlled so that its frequency does not exceed a value of 1/2 the sampling rate. The usual way to do this is with a multiple stage “brick wall filter”. A conservative design will not use a bandwidth equivalent to the limit stated above. It will instead stop the analysis well before the limit is reached. In the present system, therefore, the upper frequency limit is set at 8000 Hz, even though the theoretical limit is 12800 Hz.

Aliasing shows up as a generation of random or non-random dot patterns in the sampled data points, and occurs when the signal can take a number of excursions between samples. This aliasing in an FFT will produce a number of components in the low frequency portion of the spectrum that are really not there. It is also desirable to eliminate the high frequency components from the signal generator portion of the system. A brick wall filter is used there also.

1.2.1.3 Noise Reduction

The effects of ambient or hearing aid noise can be reduced by the use of signal averaging because the sampling process is exactly synchronized with the signal generator.

Noise reduction averaging is done in steps of 2, 4, 8, and 16. The process is done by use of an averaging buffer. The data is added to the data already in the buffer used to create the last spectral display in a ratio of 1/2, 1/4, etc., depending on the averaging called for. The result of the addition is then divided to get a properly scaled number. The effect of the non-synchronous noise is thus reduced because of the averaging process.

Averaging does not slow down the display process, but does slow down the effect that an acoustical change will cause on the displayed waveform.

Changes in the phase of signals will also show up if averaging is being used. The change of phase is accomplished by movement of the hearing aid in a sound field while the measurement is in process. The effect of phase changes is a dropout of the signal and an eventual recovery to the correct level when the motion has ceased.

2. SPECIFICATIONS

2.1 Electronics Module

2.1.1 Frequencies

Accuracy: within 1 percent

Composite Mode Frequencies: 200 Hz through 8000 Hz in 100 Hz intervals. These frequencies are presented simultaneously.

Sine (manually controlled) Frequencies: 100 Hz through 8000 Hz in 100 Hz intervals. The selected frequency alone is presented.

Sine Sweep Frequencies: 200 Hz through 8000 Hz in 100 Hz intervals, except that the following frequencies are omitted: 5700, 6100, 6200, 6400, 6600, 6800, 6900, 7000, 7200, 7300, 7400, 7600, 7700, 7800 and 7900. The frequencies are presented sequentially starting with 200 Hz.

Averaging Option frequencies:	1000,	1600,	and 2500;	or
(Sine mode only, user choice	800,	1600,	and 2500;	or
of among 6 sets of 3	1250,	2000,	and 3150;	or
frequencies)	1600,	2500,	and 4000;	or
	2000,	3150,	and 5000;	or
	500,	1000,	and 2000.	

2.1.2 Amplitudes in SPL

Composite Mode:
Speech Weighting: Response has flat amplitude for low frequency components; a slope of 6 dB/octave starts at the frequency of 900 Hz, which is 3 dB down. Amplitudes of individual components are not read out. Available RMS amplitudes are from 40 through 90 dB SPL in 5-dB steps.

Flat or White Noise Weighting: Each frequency component has equal amplitude. Amplitude is calibrated and presented at component level from 30 through 80 dB SPL in 5-dB steps. RMS source amplitudes are displayed (and are 19 dB higher than component amplitudes).

Sine Mode: 50 through 100 DB in 5 dB-steps.

2.1.3 Source Output Amplitude Accuracy (all modes)

Within 1 dB from 300 to 5000 Hz, all others within 3 dB; after leveling.

2.1.4 Crest Factor of Composite Signal

Less than 12 dB (4 to 1). Crest factor is the ratio of peak to RMS signal amplitudes.

2.1.5 Telecoil Drive

When the 6500 CX is operated in Coil mode (press COIL), flat weighted composite or pure tone operation is allowed.

	Electrical output	**field strength**
Normal operation:	0.444 mA	10 mA/meter
ANSI S3.22-1996:	1.404 mA	31.6 mA/M

Note: When the ANSI S3.22-1996 measurement option is run, the current is automatically increased.

Two coil types are now available:

Loop	**Description**	**Equivalent**
Square loop:	6020 sound box or 18" square TCOIL loop.	Room loop system
Wand:	Hand held small loop.	Telephone

The 18” square loop and the wand are connected by plugging in their cord to the RCA jack located in the side of the 6020 sound chamber.

2.1.5.1 New ANSI S3.22-1996 Coil Operation.

The new ANSI S3.22-1996 calls for the use of a small coil, which the wand fulfils. It is operated at a 10 dB higher current level. This is achieved by setting the current drive up to 1.4 mA. The standard also allows the optional use of the larger coil built into the 6020, but also at a 10 dB higher level. When the wand is removed from the jack, the current is diverted to the built-in coil, which now delivers 10 dB higher current.

2.1.6 Digital Readout of SPL

Frequency Range:	100 through 8000 Hz
Range:	From 0 through 150 dB
Resolution:	0.1 dB
Type:	True RMS

Accuracy:	Within 1.0 dB plus or minus 1 digit from 300 to 5000 Hz, within 2 dB plus or minus 1 digit all other frequencies.
Noise Tolerance:	5 dB (Prescaler range hysteresis, controlled by 6500-CX CPU)
Measurement Microphone Equivalent Input Noise:	Less than 50 dB SPL RMS or 30 dB SPL for measurements of frequency components in flat weighted composite mode.
Noise Reduction:	Averages the measured signal in synchronization with the signal generator by the factor chosen. Noise reduction averages of 2, 4, 8, and 16 times are available. Noise will be reduced by the inverse of the square root of the factor chosen. (0.7, .50, .35, .25 respectively.)

2.1.7 Battery Current Measurement

(See Appendix B of ANSI S3.22-1982)

Readout Range:	0.00 to 25.00 mA
Available Current:	Greater than 50 mA
Accuracy:	Within 3% of full scale plus or minus one digit
Zero adjust:	Automatic (Remove battery pill then press 6500-CX LEVEL button.)
Resolution:	0.01 mA
Voltages supplied:	1.5 (silver), 1.3 (mercury and zinc air)
Voltage Accuracy:	Within 15 millivolts
Resistance Accuracy:	(+/– 6% +/– 0.5 ohm)

Battery resistances simulated (measured on battery pill):

Battery Size	Chemistry	Volts	Resistance
10A/230		1.3V	11.7 ohms
675	Mercury	1.3V	5 ohms
675	Zinc/air	1.3V	3.5 ohms
13	Silver	1.5V	8 ohms
13	Mercury	1.3V	8 ohms
13	Zinc/air	1.3V	6 ohms
312	Silver	1.5V	10 ohms
312	Mercury	1.3V	8 ohms
312	Zinc/air	1.3V	6 ohms

[Engineering note: 1 ohm battery pill resistance plus 0.7 ohm circuit resistance is included in the above table.]

2.1.8 Harmonic Distortion Analyzer

Selections available:	2nd, 3rd, total (2nd+ 3rd), or [none]
Resolution:	0.1 percent
Readout units:	Percent (%). Readings are calculated with respect to total signal levels.
Manual mode frequency range:	100 Hz intervals 400 through 2500 Hz
Manual mode input range:	Up to 100 dB SPL
Sweep mode frequency range:	100 Hz intervals 400 through 1900 Hz
Sweep mode input range:	Up to 85 dB SPL
Accuracy:	Within 10 percent with respect to total percentage measured at signal levels of 80 dB SPL and above.

2.1.9 Attack/Release Time

Range:	2 to 2000 mS
Accuracy:	10% or 2 mS, whichever is larger
Resolution:	1 mS
Frequency:	2 kHz (ANSI) 1.6 kHz(IEC)

2.1.10 Power

Selectable:	100 VAC within 10% 50/60 Hz 120 VAC within 10% 50/60 Hz 220 VAC within 10% 50/60 Hz 240 VAC within 10% 50/60 Hz
Power requirements:	50 watts

2.1.11 Safety

A sample 6500-CX was tested by ETL. The 6500-CX is listed by ETL to IEC60601-1. The listing is valid only if all other mains connected equipment connected to the electronics module meets IEC60601-1. An individual 6500-CX must meet all of the safety requirements in order to bear the ETL sticker.

Safety Earth (PROTECTIVE GROUND) leakage current: less than 100 microamps

CHASSIS to MAINS PLUG resistance: less than 0.1 ohm

The 6500-CX remote module and probe mic are exempt from the 0.1 ohm requirement since they do not contain mains circuitry.

Hipot test: 1480 VAC, performed on each 6500-CX.

2.1.12 Electrostatic Discharge and Electromagnetic Susceptibility

A sample 6500-CX was tested by ETL and passed:

IEC801-2	ESD Susceptibility
IEC801-3	Radiated Susceptibility
IEC801-4	Conducted Susceptibility
EN50082-1	European Community Generic Immunity

2.1.13 Electromagnetic Emissions

A sample 6500-CX was tested by ETL and passed:

EN55011, Group 1, Class A	European Community emission limits for industrial, scientific, and medical equipment.

2.1.14 Altitude

Operating: 0 to 7500 feet (0 to 2286 meters)
Shipping: 0 to 50000 feet (0 to 15240 meters)

2.1.15 Humidity

Operating: 5 to 90 percent relative humidity (non-condensing)
Shipping: 5 to 90 percent relative humidity (non-condensing)

2.1.16 Temperature

Operating: 15 to 35 degrees Celsius (59 to 95 degrees Fahrenheit)
Shipping: 0 to 70 degrees Celsius (32 to 158 degrees Fahrenheit)

2.2 Video Display Module

Video Display Board:	061-0121-01
Video Display Unit:	VGA Monitor, either color or black and white. Type of monitor is sensed by the 6500-CX on power up.

Alternate Video Display Unit:	Composite video monochrome display, (Old 6500 analyzers) 60 Hz display rate. The video board used with the 6500 (061-0021-xx) and the RCA phono jack output connector are used with this type of display unit. CPU BOARD upgrades to 6500-CX CPU are thus possible with the older 6500 analyzers.
Video Output Connector:	High Density 15 pin D receptacle.
Display format:	320 pixels wide x 210 high
Colors:	Five (including background) are presented during the display of graphs and alphanumeric information.

Operator chosen colors: Color sets are chosen on power up by using the general setup menu (b-=bright; m-=medium; d-=dim).

Color Monitor:

Use	Default	2nd	3rd	4th	5th
Background	black	black	d-cyan	d-blue	d-white
1st curve	b-white	b-green	b-yellow	b-red	b-white
2nd curve	b-red	b-red	b-red	b-yellow	b-orange
Text 3rd curve	b-green	m-white	m-white	m-white	m-cyan
Grid 4th curve	b-blue	m-cyan	m-cyan	m-cyan	b-magenta

Monochrome Monitor: Default is bright pixels on black; black pixels on white background can be chosen.

2.3 Printer

Printer type:	Thermal
Paper type:	Heat sensitive
Paper width:	2.36" (60mm)
Print format:	320 dots over a 2.08" wide path
Aspect ratio:	1 cm per 10 dB printed graphs. 50 dB vertical per decade frequency scaling within 3 percent.

Digital and alphabetical information also displayed.

Time to print contents of CRT screen:

Composite mode:	Less than 8 seconds
Sine mode:	Less than 8 seconds
JIS option:	Less than 19 seconds
Other options:	Less than 14 seconds

2.3.1 Alternative Printer

For upgrades from 6500 or 6500-C to 6500-CX, the old 6500/6500-C printer and Printer Board are compatible with the 6500-CX. The old printer will be slower than the 6500-CX printer. Note that the two printers use different widths of thermal paper.

Paper width:	2.25" (57mm)
Print format:	100 dots over a 2" (51mm) wide path

Time to print contents of CRT screen:

Composite mode:	Less than 17 seconds
Sine mode:	Less than 17 seconds
JIS option:	Less than 45 seconds
Other options:	Less than 35 seconds

2.4 Sound Pressure Chamber

Type:	FONIX FC6020
Test Area:	6" x 3" x 1.5" deep (15.5 X 7.5 X 4 cm)
Internal Acoustical Reflections:	SPL at test point will change less than 3 dB above 1 kHz, when lid is raised (without feedback compensation)
Ambient Noise Isolation:	45 dB at 1 kHz (Allows THD measurement to within 3 % at 60 dB source level and a 60 dB ambient)

2.5 Physical Description

2.5.1 Electronics Module

Enclosure Color:	Beige with gray control panel and black trim
Net Size:	17.5"W x 6.5"D x 14.75"W (44.5 x 16.5 x 37.5 cm)
Shipping size:	23.5"W x 19"D x 11"W (59.7 x 48.3 x 27.9 cm)
Net Weight:	21 Lbs. (9.53 kg)
Shipping Weight:	29 Lbs. (13.15 kg)

2.5.2 Video Display Module (Samtron)

Enclosure Color:	Beige
Net Size:	13.75"W x 14.5"H x 14.75"D (34.9 x 36.8 x 37.5 cm)
Shipping Size:	18"W x 18"H x 18"D (45.7 x 45.7 x 45.7 cm)
Net Weight:	25 lbs. (11.33 Kg)
Gross Weight:	30 lbs. (13.61 Kg) gross

Includes cable to connect to electronics module

2.5.3 Sound Chamber

Color:	Beige
Net Size:	13.5"W x 18"H x 11.5"D (34.3 x 45.7 x 29.2 cm)
Shipping Size:	16.5"W x 22"H x 16.5"D (41.9 x 55.9 x 41.9 cm)
Net Weight:	33 lbs. (14.97 Kg)
Shipping Weight:	37 lbs. (16.78 Kg)

2.5.4 Accessories (No Probe)

Shipping Size:	14"W x 12"D x 5"H (35.6 x 30.5 x 12.7 cm)
Shipping Weight:	4 lbs. (1.81 Kg) gross

2.5.5 Accessories (Including Probe)

Shipping Size:	27"W x 17.5"D x 8"H (68.6 x 44.5 x 20.3 cm)
Shipping Weight:	17 lbs. (7.71 Kg)

2.6 Total System Shipping Weight

100 Lbs (45.36 Kg) (no probe)
113 Lbs (51.26 Kg) (with probe)

2.7 Total System Shipping Volume

17,573 cu. in. (287,970 cc)

2.8 Performance Options

ANSI: Performs all measurements defined in the hearing aid test standard, ANSI S3.22-1982. Includes the battery voltage module and telecoil.

IEC: Performs all tests outlined by the hearing aid measurement standard, IEC 118-7. Includes battery voltage module and telecoil.

AVG: Measures, in Sine Mode only, the response at 1, 1.6 and 2.5 kHz and displays a computed average of the measurement. Other frequencies may be chosen with use of menu control.

0/60: Cycles the input level to “OFF”, to 60 dB SPL, and back to “OFF” when pressed.

RBX: Measures the battery current and attack and release times of a hearing aid according to the format specified in the ANSI S3.22 standard.

GAIN: Measures the gain instead of the absolute SPL from a hearing aid by subtraction of the input signal level from the output.

MULTI: 4 of the following curves may be selected for display simultaneously: REF 1—REF 9; CRV 1—CRV 4; in both composite and pure tone modes. One curve can be subtracted from another and the result displayed. Any curve may be moved to another multi curve storage location. Two curves can be displayed with dual scaling.

JIS: Performs tests in accordance with the Japanese hearing aid standard. Both 2 cc (HA-1 and HA-2) and FONIX MZ-1 and MZ-3 couplers (corrected to give results as from Zwislocki type couplers) can be used. Attack and release times can be measured. Includes battery voltage module.

PROBE: Allows measurement of canal resonances, insitu hearing aid responses and insertion gain responses. Includes special sound field frequency response leveling routine. Allows the input of a target frequency response that can be displayed simultaneously with the measured insertion gain. Also allows input of audiometric data and selection of a gain formula for generation of the target curve. Allows display of curve data.

RS232 COMPUTER INTERFACE (RS232 OPTION): Uses 25 pin female D subminiature connector. Connected as DTE (data terminal equipment).

RS232 AUXILIARY INTERFACE (reserved for future options): Uses 9 pin male D subminiature connector. Connected as DCE (data communications equipment).

2.9 6500-CX Probe Option Specifications

(Using 061-0088-03 or 061-0088-04 Quik-Probe Preamp Board—these versions include crosstalk improvements)

2.9.1 Electrical Characteristics

2.9.1.1 Quik-Probe Microphones

Probe Microphone

Maximum Input:	Greater than 140 dB SPL at 1000 Hz
Noise Level:	Less than 55 dB SPL
Frequency Response:	250 Hz to 8 KHz +/– 2.5dB
Crosstalk from Ref Mic:	Less than –42 dB
Crosstalk from M1550E:	Less than –75 dB
Crosstalk to M1550E:	Less than –66 dB

Reference Microphone

Maximum Input:	Greater than 140 dB SPL
Noise Level:	Less than 50 dB SPL (typically 43 dB SPL)
Frequency Response:	100 Hz to 8 KHz +/– 3dB
Crosstalk from Probe Mic:	Less than –80 dB
Crosstalk from M1550E:	Less than –70 dB
Crosstalk to M1550E:	Less than –90 dB

Internal Signal Level

Remote module to 6500-CX cable (typical, not guaranteed): 30 mV p-p = 100 dB SPL

2.9.1.2 Field Speaker Amplifier

Output Power:	1 watt RMS continuous, 3.0 Watts RMS for brief periods
Load Impedance:	8 ohms
Total Harmonic Distortion:	Less than 0.5%, typically 0.1%
	Short circuit protection:Amplifier IC is self protected, however after a few seconds of short circuit operation, 6500-CX power supply resistors R18 and R16 may burn.
Thermal Protection:	Amplifier IC is internally thermal protected. Heat sink capacity is not as great as possible amplifier thermal output.
041-1504-00 Field Speaker Output:	Greater than 90 dB SPL tone. Greater than 90 dB SPL composite

2.9.1.3 Headphone Amplifier

Monitored channel:	Probe microphone
Short circuit duration:	Indefinite
Output impedance:	600 ohms (set by resistors)
Headphone type:	Stereo or mono, using 2 or 3 conductor 1/4 inch phone plug
Usable headphone impedance:	32 ohms to 600 ohms (intended for Walkman style headphones)
Open circuit output voltage at clipping:	9 volts peak
Open circuit gain from probe microphone:	100 dB SPL = 1 volt rms, max gain

2.9.2 Physical Characteristics

Dimensions, Remote Module, less cable:	1.7 x 4 x 7.5 inches (4.32 x 10.16 x 19.05 cm)
Net Weight, Remote Module with cable, less accessories:	1.43 Lbs (0.65 kg)
Length, Remote Module Cable:	10 feet (305 cm)
Length, Quik-probe microphones cable:	10 feet (305 cm)
Reference microphone dimensions:	0.55" (14 mm) diameter 1.3" (33 mm) long
Probe microphone dimensions:	.395" x 1.3" long
Probe tubing dimensions:	.95 mm (0.037") o.d. typical 0.5 mm (0.020") i.d. typical 76 mm (3.0") long
Probe tubing material:	Silicon rubber

3. SPECIFICATION TEST PROCEDURE

3.1 Frequency Accuracy

Instrument required: Frequency counter accurate to 0.1 percent and capable of measuring 1000 Hz.

Turn on the 6500-CX and press RESET. Press SINE/COMPOSITE. Set the amplitude to 100 dB SPL. Connect the frequency counter to the source output at the point where it connects to the sound chamber.

The reading of frequency should be as read out on the CRT within 1 percent.

3.2 Frequence Response

Instrument required: Precision sound level meter with 1/2 inch condenser microphone. Response set to flat frequency response.

Turn on the 6500-CX. Press RESET. Be sure that Noise Reduction is turned off. Press SINE/COMPOSITE to put the 6500-CX into pure tone mode.

Place the precision sound level meter microphone at the reference point in the sound chamber; place the M1550 microphone so that its grill is facing the sound level meter's grill. Set the level to 90 dB SPL.

Starting at 100 Hz, measure the RMS levels at the reference point with both systems. They should agree within the tolerance of the measuring meter plus the tolerance of the 6500-CX response.

3.3 Attenuator and Scaling Accuracy

Equipment required: Precision A.C. voltmeter.

Turn on the 6500-CX. Press RESET. Be sure that Noise Reduction is turned off. Press SINE/COMPOSITE to put the 6500-CX into pure tone mode.

Set the frequency to 1 kHz. Patch the electrical drive signal from the source output back into the microphone input and into the input of the precision AC voltmeter as well.

Note the input level in dB SPL, the measured voltage and the output level in dB SPL. Change the level in 10 dB increments and note that the levels all change by 10 dB increments. With respect to the measuring voltmeter, make sure that all levels track within the needed tolerance.

CAUTION: Make sure that an adequate signal to noise ratio is maintained. This can be important in getting good measurements, especially at low signal levels.

An attenuator may be needed to reach low signal levels. This may be formed by use of a series resistor and a shunt resistor of 1000 ohms across the microphone input. A high resistance drive to the microphone input should be avoided because of shunt capacitance that is added to this circuit for purposes of RF interference rejection.

3.4 Sound Level at Reference Point

Use the same setup as called for in 3.2 for measuring frequency response.

Turn on the 6500-CX. Press LEVEL. Be sure that Noise Reduction is turned off. Press SINE/COMPOSITE to put the 6500-CX into pure tone mode.

Press the amplitude up button to set the level to 90 dB SPL. Set the frequency at first to 200 Hz and then advance the frequency at intervals to 8000 Hz and check to see that the SPL as measured by the sound level meter is 90 dB SPL within the tolerance specified.

3.5 Crest Factor of Composite Signal

Equipment required: Precision A.C. voltmeter with true RMS output measurement. Oscilloscope.

Turn on the 6500-CX. Press RESET.

Set the source output to 90 dB SPL RMS, speech weighted composite signal (either weighted gain or weighted power modes). Connect both the voltmeter and the oscilloscope to the signal output. Measure the RMS voltage present in the output. Note this figure. Now compare the peak voltage (as compared with 0 VDC) from the oscilloscope trace with the true RMS reading. The ratio should be less than the specified value.

3.6 Telecoil Drive

Equipment required: Precision A.C. current meter true RMS output measurement.

Turn on the 6500-CX. Press RESET. Press COIL.

Place the current meter in series with the telephone coil. The current should read 0.444 mA. within the tolerance specified. Press COIL again. Press MENU and then COIL. Set frequency to 1 kHz for measurement. Press MENU again and then press COIL to activate measurement at 1 kHz.

Measure current flow at 1 kHz to be within specified tolerance of 0.444 mA.

3.7 Battery Current Measurement

Equipment required: Precision D.C. voltmeter. Precision 1.5 k ohm resistor. Precision 100 ohm resistor.

Turn the 6500-CX on. Measure the voltage at the battery voltage module output to be 1.5 volts while in the silver positions and 1.3 volts while in the mercury and zinc air positions. Check to see that the measured voltage is within the specified tolerance.

Connect the 1.5 k ohm resistor at the output terminals of the battery voltage module. Set the module to silver, type 675 (76). Run the RB option or the ANSI or the IEC option to measure the battery current. See that the reading is 1 mA within the specified tolerance.

Connect the 100 ohm resistor across the output terminals. Repeat the above test. The new reading should be 14.4 mA within the tolerance specified.

4. CIRCUIT DESCRIPTION

Logic Notation
Some logic circuit inputs and outputs operate with positive true logic. A "+" voltage at such a point is equivalent to a "one." Other inputs and outputs operate just the opposite, with negative true logic. The circuit descriptions which follow label negative true inputs and outputs by a "\."

A high speed data bus is present at the top of many of the circuit boards used. The bottom bus connector is used for analog signals, power, and printer digital drive.

General Description
The following boards are used in the 6500-CX:

a. I/O
b. CPU
c. Signal Generator
d. Digitizer
e. Video
f. Printer
g. Power
h. Main Panel
i. Printer Switch

The I/O BOARD contains several circuits, most of which are used for communications with the outside world. They are:

a. An RS-232 port circuit
b. Input port to let the CPU see how to set up the RS-232 and to read the state of the push button latches. The push buttons are connected to a series of eight latches which hold the push button values until the CPU reads them.
c. An output port to light up LEDs on the front panel, to reset the push button latches, and to provide printer read and write pulses
d. Byte reversal port to aid in FFT calculations
e. A port to drive the printer

The CPU BOARD contains a 68000 microprocessor. This processor was chosen to allow fast data calculations needed for the FFT process. It handles all control of the 6500-CX, and has up to 128k bytes of PROM and 32k of RAM. It also contains interrupt input circuits.

The SIGNAL GENERATOR BOARD contains the circuits for conversion of a 256 12-bit word map to an analog signal. The map is loaded to this board from the CPU board. A 5 dB per step attenuator is also built onto the board and is controlled by the CPU. The output signal is delivered to the lower bus for amplification by the power amplifiers. A filter is also located on this board to remove the frequency components above the 8 kHz top frequency.

The DIGITIZER BOARD is also controlled by the CPU. This board contains a CPU controlled prescaler and a brick wall filter to prevent aliasing.

Digitizing is done by means of a 256 sample system and can be synchronized to the signal generator, if desired. The sampling rate is 25.6 kHz, the same rate used by the signal generator.

The 12-bit accurate sampled data is stored in RAM and can be read as desired by the CPU. When performing attack and release measurements, the sampling is done without synchronization with the signal generator.

This board also contains battery voltage generation and current measurement circuits. The amplitude of the current is changed to a voltage that is switched to and measured by the 12-bit A to D converter.

The VIDEO BOARD contains the circuits that generate a bit mapped graphical image by outputting a composite video signal to the external CRT monitor. Through time-sharing, the CPU board has direct access to the RAM on this board. The circuits then read the RAM and generate the display. The general format of the display is that of a 320 wide by 210 high bit mapped picture.

A printout of the CRT is made by first printing the top 100 lines of the screen, followed by the bottom 100. The last 10 lines are not normally printed.

The PRINTER BOARD drives the printer. The combination creates hard copy of the data on the screen of the CRT. It also is used to print single lines of data as well as a header that can be placed at the start of a graphical printout.

The printer contains a printhead with a single row of 100 dots that can be heated to print dots on thermally sensitive paper. A special regulated 25 volt power supply is included on the printer board to drive the print head dots as well as the print feed drive motor.

Controlling data is sent to the printer in 4-bit “nibbles” by the use of a special port on the I/O board. This print system is the same one used by the well tested FONIX 5500-Z. Because the new processing elements require both + and – 12 volt supplies, the POWER BOARD is modified to provide unregulated + and – 18 volts to the

power bus. Power is regulated on the individual boards for best isolation and noise reduction. –18 volts is supplied on pin 12 of the lower bus. +18 volts is supplied on pins 49 and 50. The audio power amplifier located on this board is also used for speaker drive, as on the 5500-Z. Unregulated + and –10 volts are also supplied on the power bus on pins 47, 48 and 45, 46, respectively.

On the MAIN PANEL BOARD, silicon rubber DPST button elements are used along with LEDs for state indications.

The PRINTER CONNECT BOARD with its switches and LEDs is an extension of the main panel board and is connected to it with a cable.

4.1 Addresses and Control Ports

4.1.1 Addressing in the 6500-CX

This is the 6500-CX memory map. Not all addresses are fully decoded.

Address (HEX)	6500-CX Board:	Function
000000-07FFFE	CPU Board:	EPROM
080000-0BFFFF	CPU Board:	RAM
0C0000-0C1FFF	CPU Board:	timekeeper RAM, non-volatile
100000	I/O Board:	UART
100010	I/O Board:	LED port, print control strobe, keyboard control
100020	I/O Board:	print data strobe
100040	I/O Board:	byte reverse
100080	6500 Interface:	probe control port
100082	6500 Interface:	probe keyboard port
100101	Video Board:	video control port
200000-203FFF	Video Board:	video RAM
400000	Digitizer Board:	control port
400000	(same) Signal Generator:	control port
800000-8001FE	(read) Digitizer:	RAM
800000-8001FE	(write) Signal Generator:	RAM
FFF000-FFFFFF	CPU Board:	CPU configuration registers

4.1.2 Control Port Addresses

Output and input port addresses from 100001 through 10000F are for the control bytes for the RS-232 chip and for retrieval of information.

Input port 100010 is the address for the push button and mode select switch word. Push buttons take the lower 8 bits.

Output port 100010, bits 0 through B, is the address for the LED driver output port (1 = light the LED). Bit D is the I/O read and Bit E is the I/O write strobe for the printer drive (0 = strobe). Bit F is the reset bit for the push buttons (0 = reset).

Output port 100021 is used for the printer drive. Coding of the data is as follows:

Bits 0 through 3 is the data to the printer

Bits 4 through 7 is the address of the printer latch

After the data is written to the port, the I/O write pulse must be sent by setting bit E of address 100010 to 0 momentarily.

100041 is the address of the byte reversal port. A byte written to this port, if read out again, will be in reversed order.

Control Port Use (400000)

Bit	Input Port	Output Port
0	State of LSB of sampler timer.	1 = synchronous sampling 0 = nonsynchronous sampling
1	State of sampler. If 1, the sampling process has been done and data may be read out.	Normally 1. When set to 0 momentarily, the sampler is armed and starts to sample the input waveform.
2	Battery type port.	0 = sample battery current. 1 = sample the waveform.
3	Battery type port.	Not used
4		1 = set the prescaler gain 40 dB
5		Set prescaler gain to 20 dB
6		Set prescaler gain to 10 dB
7		Not used
8 9 A B		Bits 8 through B form an address nibble to control gain of the signal generator amplifier. 0 is the lowest controlled gain, or 50 dB SPL output. A gives a gain for an output of 100 dB SPL. B through F turn the generator off.
C		Bit C controls the 6 dB/oct slope rolloff of the signal generator board (0 = flat)

Table 4.1

4.2 I/O BOARD (061-0029-XX)

4.2.1 Push Button Latches and RS-232 Setup

The push buttons are accessed by the CPU through memory mapped location 100010. They comprise the lower eight bits of a 16-bit word. Buttons are read as either single bit or two bit settings of the latches according to the map in table 4.2.1. It should be noted that the map is of pin connections of the interface connectors, rather than bit addresses. A bit address of 0 is routed to pin 1; Bit 1 to pin 2, etc.

One pole of each switch and each LED is connected to ground. Other poles are connected to pins on the 26-pin connector (J1) on the front panel board (060-0019-XX) or the 14-pin connector on the switch board (060-0017-XX). See also Table 4.2.1.

Lines 1 through 8 of J4 carry the push button switch connections to the two 4-bit latches, (U3J and U3K). The latches are reset when a 1 is written to the F line of the LED port (U4D).

The operator can set up the RS-232 port by setting the DIP switches on the I/O board. The program reads the settings as the high order bits of the 16-bit word accessed at location 100010.

Decoding of the location is handled by address lines A20 and A4 through 74LS00 (U3A) and control lines AS\, UDS\ and LDS\ through 74LS260 (U1J) and 74LS00 (U1K) working on the R/W\ line.

4.2.2 RS-232 Control

RS-232 control is accessed by odd addresses 100001 through 10000F. Control is decoded by 74LS260 (U2A) preventing access if address lines A4 through A8 are high. A2O is anded with U2A output at 74LS00 (U3A); processor signals AS\ and LDS\ are anded in through 74LS260 (U1H).

When data is received by the RS-232 8250 chip (U3M), an interrupt is sent to the CPU via the 74LS04 (U2J). When the 8250 is not inserted, the input to the 74LS04 (U2J) is tied to ground to keep the interrupt from occurring.

The 2 MHz clock for the 8250 is made by counting down the 8 MHz system clock using two sections of 74LS73 (U1L).

6500-CX Switch Pattern

J1	Switch	J1	Switch
1	relative (S13)	3-7	I/O (S24)
1-2	sine/composite (S1)	3-8	RBX (S20)
1-3	weighting (S2)	4	option 4 (S7)
1-4	harmonic distortion (S5)	4-5	multi (S16)
1-5	noise reduction (S4)	4-6	insitu (S17)
1-6	cursor (S12)	4-7	probe (S26)
1-7	coil (S30)	4-8	option 1 (S10)
1-8	menu (S9)	5	amplitude up (S21)
*2	feed	5-6	ANSI (S14)
*2-3	print CRT	5-7	IEC (S15)
*2-4	print line	5-8	option 2 (S11)
*2-5	title	6	amplitude down (S22)
*2-6	level	6-7	option 3 (S6)
*2-7	label	6-8	continue (S29)
2-8	start (S28)	7	frequency up (S25)
3	freeze (S8)	7-8	graph/data (S31)
3-4	0/60 (S19)	8	frequency down (S18)
3-5	average (S23)	10	reset (S3)
3-6	gain (S27)		

LED Assignments		Connections Between Connectors		
J1	LED	J1 (26-pin) 060-0019-XX	J2 (9-pin) 060-0019-XX	J2 (14-pin) 060-0017-XX
11	super/sine	2	2	1
12	graph/data	3	3	13
13	2nd harmonic	4	4	2
14	3rd harmonic	5	5	12
15	ANSI	6	6	3
16	IEC	7	7	11
17	gain	9 (gnd)	1	14
18	weighting	22	8	4
19	noise reduction	26	9	10
20	option 1			
21	option 2			
*22	label			
23	option 4			
25	option 3			
*26	power			

*Switches and LEDs on switch board (060-0017-XX)

Table 4.2.1
Switch and LED connections

4.2.3 LED and Push Button Latch Reset

The same decoding is used here as for the push button and RS-232 mode reading, but with the R/W\ logic inverted by (U2K) and (U1K). Bits 0 through A are used for LED drive. Bit F is used as a reset bit for the push button latches. Bits D and E are used to supply strobes to the printer board.

4.2.4 Bit Reversal Port

Address 100040 is used as a port to provide bit reversal. Writing a lower order byte to the word (or a byte to address 100041) will latch data to 74LS373 (U3B). This data can now be read out at the same address in reversed order through 74LS373 (U2B).

A special DTACK\ signal is generated by use of the 2N2222 transistor (Q1). This is done to speed the access time to this data.

4.3 CPU Board (061-0122-XX)

4.3.1 General Operation

The processor chosen is the 68331, which contains a number of circuits that are often handled by external logic devices. This processor is a newer member of the 68000 family. It allows high processing speed because of a high clock rate (16 MHz) and fast internal operation.

The CPU board incorporates an RS-232 interface on board which is available for extra operations.

PROM and RAM elements of up to 4 megabits each (256K bytes) may be used.

A new battery backed up RAM and real time clock is present on the board to allow storage of operating parameters and the readout of the time and date of the measurement.

4.3.2 68331 Processor

The 68331 processor runs at a clock rate of 16 MHz. It directly accesses memory elements on the CPU board, but is isolated from the external 6500 bus by buffers U1,3,5,7, and 8. These buffers handle the bidirectional data bus (U3,5), the address bus (U1,7,8) and the data strobe signals, respectively. The address line A23 and the 8 MHz system clock are buffered but not switched by U8. The address and address strobe lines are switched off at the time an interrupt is processed (see 4.3.2.3 for interrupt description).

4.3.2.1 Addressing

A set of programmable chip select lines are available from the 68331. These are CSBOOT\ for PROM addressing; CS0, 1, and 2 for RAM; and CS6 for the real time clock and battery backed up RAM. These CS signals make the selection and drive of the memory elements very simple and straightforward.

The address lines A20, A21, A22 and A23 are also programmed as chip select addresses for 6500 device operations. A circuit is also added (U10, a PAL) to decode processor lines in order to generate the needed UDS\ and LDS\ data strobes which are used by the circuits on other boards in the 6500. These signals are not provided by the 68331.

It is interesting to note that an A0 address line is available and is used for battery backed up RAM addressing.

4.3.2.2 Wait State Processing

The wait periods are internally programmed so that when a PROM, RAM, or other device is sent a read or write command the proper wait time to assure good data reception is used. Some circuits external to the CPU board supply their own wait state timing. These circuits use the DTACK\ line to signal the end of the wait period.

4.3.2.3 Interrupt Handling

Programmable interrupt handling circuits are all contained inside the 68331. All interrupts can be disabled though program control. Interrupts are as follows:

CPU Pins	Interrupt level
IRQ1 Printer	(level 1, lowest level)
IC2 Keyboard (Not used)	(level 2)
IRQ4 RS-232 (from I/O board)	(level 3, not set)
RS-232 (CPU internal)	(level 4)
IC1 O set	(level 5)
IRQ6 Keyboard Reset	(level 6, highest level)

Interrupts are under program control, and can be disabled, starting at the lowest level first.

When an interrupt is processed, all address lines are affected; they are therefore disconnected from the active 6500 circuits by turning off the interface buffer chips (U1,7,8).

4.3.3 Clock

The clock is supplied by a crystal oscillator chip, Y1, which runs at 32 MHz. The 16 Mhz clock is supplied by counting down the 32 MHz by two in U12B. Sixteen MHz is delivered to the CPU chip, which then is used to supply a 16 MHz clock to U12A, which further counts it down to 8 MHz for system use. This system clock is buffered through U8.

4.3.4 Power on Reset

This function is supplied by U11, which forces a delay of 250 milliseconds minimum after the power supply voltage has risen to 5 volts within 5 percent. An out of tolerance voltage dropout will force a RESET\ signal to the CPU chip, shutting down operation.

A further function is that of a forced reset by shorting pin 1 to ground through an external switch closure. This feature can be used for debugging purposes.

The chip is also a watchdog circuit. This function is disabled by running the 8 MHz clock signal to the watchdog input.

4.3.5 Control Lines

Several control signals are needed for proper operation of the 6500 circuits. They are upper data strobe (UDS\), lower data strobe (LDS\), address strobe (AS\) and the read write signal (R/W\). A0 is not placed on the 6500 address bus, but is replaced by the UDS\ and LDS\ signals for 8 and 16 bit operations.

Two of the signals, AS\ and R/W\, are supplied from the 68331 chip. The upper data and lower data strobes must be generated by logic from signals supplied from the 68331. This is done by the use of the PAL, U10.

All of these signals are buffered through U8 onto the 6500 bus. They are switched off at the time of an interrupt process. The control of the switching process is also done through the PAL which looks at the signals from the 68331 and generates the signal ABEN.

4.3.6 PROM and RAM

The control PROM is U6. It has a 4 megabit capacity, and is read out in 16 bit words. It is read when CSBOOT\ enables the chip.

Two RAM chips (U2 and 4) are used, and may be written in 8 bit bytes or 16 bit words. CS1\ will always read the RAM in 16 bit words. CS0\ allows writing to U2 in

8 bit bytes. CS2\ writes to U4. If CS0\ and CS2\ are both exercised, a 16 bit write takes place.

All chip selects are programmable and come from the 68331.

4.3.7 Control Logic

Control logic is minimal, being mostly handled on the 68331 processor chip. Four signals are supplied by the control logic element U10. They are UDS\, LDS\, ABEN and DBEN\. UDS\ and LDS\ are upper data and lower data strobes. ABEN is a signal used to disconnect the address and control lines from the 6500 data bus. DBEN\ is used to control the 6500 data bus connection to the CPU data bus.

U10 handles the following signals supplied from the 68331 to determine the states of the four signals listed above: EBEN, SIZ0, SIZ1, A0, A20, A21, A22, A23, FC0, FC1 and FC2.

4.3.8 Battery Backed up RAM and Real Time Clock

U14 handles this function. It supplies 8K bytes of non volatile memory as well as a clock function. The top 8 bytes are filled by the real time clock, and can supply date and time functions. Access to the chip is provided by the programmable chip select line CS6\ from the 68331.

The built-in battery has an expected life of 10 years and is kept charged during periods of 6500 use.

4.3.9 RS-232 Interface

A function supplied by the 68331 is an RS-232 interface. This connection is now made directly from the CPU board and is buffered through the interface amplifier chip, U13.

The + and – 12 volts for the proper operation are supplied through U15 and U16, which regulate the voltages for the interface.

The connector J4 has the same pinout as that of the RS-232 interface circuit on the I/O board.

4.4 Signal Generator Board (061-0025-XX)

This board is designed to generate the signal that is used to test the device. The basic components are a counter, clock signal logic, data input buffers, RAM chips, 12-bit D to A converter, low pass filter, and output amplitude control.

4.4.1 Counters

The counter is used to generate the 25.6 kHz clock signal that, when counted by a factor of 256, provides the basic 100 Hz frequency of the system. The clock uses the 8 MHz clock from the 68000 processor as a source, and counts this clock successively by 13, 3 and 8. The clock frequency is thus 25.641 kHz, which is .16% high in frequency. The divide by 13 counter is formed by a 4-bit counter (U4E) with feedback to its reset input on the count of 13 through (U2E) and (U3H). The count of 3 is formed by a pair of JK flip-flops (U4F). It produces a nonsymmetrical output, which is used for timing signal generation for clocking the D to A converter. Other signals are also developed by logic elements hung on the divide by 8 counter which is formed by part of the 4-bit binary counter (U4H). These signals are used to control the operation of the A to D converter on the digitizer board.

The final count of 256 is formed by two 4-bit counters, 74LS197s (U2A) and (U2B). This part was chosen because it can also act as a buffer, passing the address from the digital bus connector through to the RAM when the 68000 wants to load data into the RAM waveform storage elements. This is done by the use of the PRESET input, which interrupts the count and connects the preset inputs to the outputs.

4.4.2 Logic

A short 1.625 uS clock pulse is derived by logic elements (U4B) 74LS08 and (U3H) 74LS21, working from the divide by 8 (U4H) 74LS93 and the clock pulse drive to the divide by 3 circuit. This pulse is used to drive the divide by 256 counter to step the address by one count at a time.

(U3H)'s output is also used to set the states of a JK flip-flop (U3F). Thus, when the clock pulse falls, the Q output of this flip-flop goes high, enabling (U3D) the 74LS00. The next clock pulse input drives a pulse through (U3D) a NAND gate and drives a RAM\ signal to latch in the next set of data for conversion by the DAC (U1E). Since this pulse is 3.25 uS later than the previous one that upped the address count on the RAM, the new data is solid.

Logic elements are also added to enable the 68000 to send data to memory locations it wishes. This is done by the 68000 first setting up the address and data on the appropriate lines, A1 to A8 and A23 and D0 to D11. Once these signals are in place,

the R/W\ line goes low and the AS\ and UDS\ and LDS\ lines are also sent low, indicating that a write is requested, the addresses are correct, and that both upper and lower data bytes are to be used. A write command for A23 is always directed to be sent to this board. A read to this line means that sampled data from the digitizer board is to be read.

Decoding is straightforward. A RW\ signal inverted by (U3E) 74LS04 and an A23 signal enable the gate (U3D) 74LS00. Arrival of AS\ low then pushes (U4D) 74LS02 output high, which enables high and low write command gates to the lower 8 and upper 4 bits of the 12-bit word. If LDS\ goes low, and if DTACK\ is high, (U4D) 74LS02 tells (U3D) 74LS00 to accept that OK from the A23 decode logic, and data is written to the lower 8 bits by pulling the W\ inputs of (U3A) and (U3B) low. Similar action works on the upper 4 bits with (U3C).

4.4.3 RAM

RAM is formed by three 2114s — (U3A), (U3B) and (U3C). The upper address lines of these chips are tied to ground, thus the upper half of the chips are unused. The four bit chips are arranged to supply storage for the twelve bits of data that arrive from the 68000 and that are read out to generate the signal.

An address is delivered from the CPU to the RAM chips when the invertor (U2E) 74LS04 has pulled the Load inputs of the (U2A) and (U2B) counters low and directed their outputs to follow input lines A1 through A8. Data is also coupled to the RAM data lines by the same logic drive line operating on (U2C) 74LS244 and (U2D) 74LS125 for the lower and upper order bits, respectively.

When the DTACK circuit on the CPU pulls DTACK\ low, the write is ended. When the CPU responds to the DTACK, the address strobe command on AS\ is withdrawn.

When the system resumes operation, the count will of course start from the last preset count given the counter chips from the address lines. Since the 68000 will probably only write to these locations when it is in the process of changing a complete RAM table of data, the disruption of signal will be a relatively infrequent affair. Programs have also been developed so that when necessary, the RAM is loaded in synchronism with the system so that only a small signal transient is generated by the load process.

4.4.4 Logic Used by the Digitizer Board

The 74LS21 (U3H) and 74LS08 (U4B) tied to the outputs of the divide by 3 and 8 counters provide a short basic clock signal labeled RAM\.

The two sections of the 74LS260 (U4A), a dual 5 input NOR, in combination with the 74LS08 (U4B), provides another signal for the A to D converter called 0SET. The

signal goes high only when a complete count of 256 has been completed and the count is about to start again. The count of 0 is anded with the clock pulse to produce the 0 set signal. These two signals then provide the A to D on the digitizer board the information needed to do synchronous sampling.

CE\ tells the A to D chip to perform a function (either read or convert). R/C\ tells it what function to perform. When R/C\ is high, a CE\ causes the A to D chip to read out the binary conversion information to RAM. When R/C\ is low, a CE\ causes the analog to digital conversion to start. Another signal, RAM\, is used to enable the RAM on the digitizer board to be written with the new set of conversion data. This also must occur a short period of time after an address change for proper RAM loading.

Timing is important on these operations because the AD574A used for digitizing takes 35 uS to perform a conversion. The clock rate is 25.6 kHz, or a period of 39 uS. Thus the timing difference between the CE\ pulses that first load the data from the last conversion to a new address in RAM and then start a new conversion must be less than 4 uS. The period of the drive to the divide by 3 circuit has a period of 1.625 uS, and its drive pulse has a width of .625 uS.

R/C\ also is used to drive the sample/hold circuit on the digitizer. A relatively narrow clock pulse of 0.625 uS is derived by using the drive pulse to the divide by 3 counter in combination with logic elements. A pair of CE\ pulses, one for reading and the other for A/D conversion, are generated by the use of a flip-flop (U3F). They are separated by 1.625 uS.

The dual flip-flop (U3F) can be thought of as a delay generator. Normally both outputs of these flip-flops are low, held there by the bias on their JK inputs. When the bias is flipped on the first one, the next pulse's trailing edge flips it high, arming the second flip-flop so that the next pulse's trailing edge will flip its output high. The second flip-flop is always trailing the first one by one pulse.

Clock pulses from (U4E) cause all the action. If the count in U4H is eight, U3Fa is biased to be triggered high. The falling edge of the first clock sets it high. U3Fa high sets the second FF (U3Fb) bias so that it can be triggered high on the second clock. The falling edge of the second pulse also causes (U3Fa) to fall because its bias has been changed. The second FF (U3Fb) is now biased to fall on the third clock pulse. hen it falls, action is terminated until the count of eight is true again. The other logic elements use the delays caused by the serial flip-flop action to generate the timed pulses, RAM\, R/C\, and the dual CE\.

R/C\ starts by being pulled high by the first clock pulse. The falling edge of this pulse sets FF1 (U3Fa) high and this FF1's output is used to extend the time R/C\

stays up. The 100 pF cap holds it up if the FF1 is a little slow in getting up.

RAM\ is generated when (U3D) is armed by FF1 and the second pulse goes high. It also causes the generation of the first CE\ pulse through (U3E) 74LS04 and (U4D) 74LS02.

The falling edge of the second pulse pulls FF1 low and terminates the R/C\ pulse. Thus when the last pulse comes through, it passes through the enabled gates (U4B and U4D) to generate the second and last CE\ pulse and starts the conversion process on the digitizer board. The falling edge of this pulse sets FF2 low again, disarming the gate.

The drive signal, RAM\, enables the RAM chips on the digitizer board to receive information from the A/D converter. It is also used to latch through the data from the signal generator RAM to generate the next programmed level. Examination of the action of the flip-flops will show that the RAM\ clock is exactly one clock cycle later than the cycle that caused an address change, making sure that the data will be solid and stable.

4.4.5 Digital to Analog Converter

All of the latch lines on the DAC811 (U1E) except the WR\ input are tied down, because the eight bit and four bit load features are not used in this design. A 12-bit word is available all at once, so the single instruction RAM\ to load the data will make a clean signal transition possible.

4.4.6 Low Pass Filter

This filter is used to remove the higher order frequency components above 8 kHz that can cause possible difficulties with the signal being processed by the 6500-CX's power amplifier and the device under test. It is formed by a series of op-amps (U1J and U1L) forming two 2-pole filter sections and one 2-pole filter, respectively.

4.5 Digitizer Board (060-0023-XX)

This board contains circuits to preamplify the incoming signals with prescaling controlled by the 68000, a brick wall filter to reduce the high frequency components above 8 kHz, a switch to allow either audio signals or battery current signals to be measured, a sample and hold circuit, an A/D converter, RAM for holding the sampled data in 12-bit words, a counter for deriving addresses for the RAM in data collection, and logic circuits to control the board. A circuit is also included that supplies a battery equivalent voltage and a current voltage converter that ranges up to –5 volts for a current drain of 25 mA. A number of signals are supplied from the

signal generator board for timing the sampling operation; look at the description for this board for their derivation.

Digitizer board logic also allows the CPU to read the RAM locations as desired, to control the gain of the prescaling amplifier, to determine the state of the A/D process, to set whether the sampling is to proceed synchronously with the signal generation or not, and to measure either input audio signals or battery current.

4.5.1 Preamplifier

The preamp is a single op-amp (U2N) TL071 with a gain of about 1.5. Gain is controlled by the 10K pot mounted on the rear panel.

4.5.2 Prescaling Amplifier

All prescale amplifiers operate in the same way. Operating the switch so that it shorts out the resistor connected to the leg of the minus input to ground effectively switches the stage's gain to the high state. Opening the switch removes the attenuation of the feedback signal and the gain reverts to unity, or 0 dB.

The first amplifier (U2M) forms a pair of 20 dB stages. The second forms a single switched 20 dB amp and a 10 dB amp (U3L).

The 2.2 uF caps (C110, 113, 122, 120) are used to keep DC offset glitches from forming and being switched into the system when the gain is changed.

4.5.3 6 dB/Octave Compensation Amp

TL071 (U2K) and 2N4293 FET (Q103) form a high frequency boost filter that can be switched in when it is desired to operate in speech weighted gain mode. The filter is formed by passing the signal through the .016 uF cap around the 11k input resistor. The output feedback resistor is also 11k, so that the gain is unity at low frequencies, but increases at a rate of 6 dB/octave at the corner frequency of 900 Hz. The gain is limited at high frequencies by the 330 ohm series resistor and the 300 pF shunt cap.

4.5.4 Logic

Logic is required to enable the system to read asynchronous sampled data such as the response of the aid in attack and release times measurements.

A logic one is provided to port (U2C) 74LS125, bit 1, when an arrival of the R/C\ pulse sets flip-flop (U4F), pin 9, high. This signal is used to tell the CPU that a sampling event has taken place and that the data has been transferred to RAM and is in the state to be read out. The act of reading out the value sends a reset pulse to (U4F), setting bit 1 low again.

In sine mode, during the loading of the signal generator, it is necessary for the CPU to know when an address change has taken place. This is done by reading bit 0 of port (U2C) 74LS125, which is connected to the low order bit of the address counter.

4.5.5 Low Pass Filter

This filter is formed by operational amplifiers U3K and U5K and is used to control the bandpass of the signal being sampled to avoid aliasing problems. It is identical in design to that used on the signal generator board.

4.5.6 Signal Switch/Sample and Hold

The sample and hold circuit is formed by 4066 CMOS switches (U2J) and (U2H). C136 and C137 are used as storage capacitors. The circuit is driven by (U3H) 3302 and flip-flop (U4F) which is clocked by the R/C\ signal from the signal generator board. In normal sampling operation, the FF drives the signal from isolation amplifier (U5H) through pin 4 of (U2J) into C136. At the same time, the voltage that was delivered to C137 is being read out by op-amp (U1H) TL071 through pin 2 of (U2H) 4066. On the arrival of the next R/C\ pulse, the switches are changed, so that now C137 is disconnected from the (U1H) op-amp input and connected to be charged by the isolation amp (U5H). The previously charged C136 is then connected to the readout amp.

Sampling operation takes place when bit 2 is set at port (U4D) 74LS373.

Battery current can be read out in the form of a negative voltage offset by setting bit 2 to 0. The low voltage resets flip-flop (U4F) and stops the sampling. At the same time, (U2H) pin 10 is connected to C136, and this voltage is permanently connected to the input of the readout op-amp (U1H) TL071.

4.5.7 Analog to Digital Converter

Analog to digital conversion is performed by the AD574A chip. It is connected to process 12 bits at a shot, and also to load these 12 bits all at once to RAM when commanded. It requires 35 uS to make a conversion. Layout around this part is extremely critical to avoid noise problems. Twelve bits is equivalent to a signal to noise ratio of 4000 to one, or 70 dB.

4.5.8 RAM

RAM is formed by the combination of three 2114 chips (U5A, U5B, U5C). They are addressed by the 74LS197 counters (U2A, U4A). Each chip stores 4 bits of the 12-bit word used by the system.

4.5.9 Counters and Control Logic

The 8 bit counter pair is formed by 74LS197s (U2A and U4A) which are used because of their preset feature, allowing the 68000 processor to control the address for readout of sampled data. These chips receive a clock signal every 39 uS from the RAM\ line, which is sent over from the signal generator board.

The signal 0SET also comes from the signal generator board. When this signal arrives, the counters are reset to 0 so that they are in synchronization with the counters on the signal generator board if bit 0 is set high on port A22 (U4D). If the bit is set low, then nonsynchronous sampling will take place. (U6A) 74LS00 supplies the control logic.

The system is designed to start synchronous sampling only when enabled by a momentary negative pulse delivered from bit 1 of the 74LS373 (U4D). This action resets flip-flops (U5F) and allows the CE\ and RAM\ pulses from the generator board to start clocking data to the RAM by way of the A/D. When the 0SET pulse comes in, the first flip-flop is clocked high. The next 0SET pulse causes the output of the first flip-flop to fall, and then the second Q\ goes low again, stopping the sampling. The sampler has thus caused a synchronous load of 256 words to the RAM, and will not restart until another pulse is received from bit 1 of 74LS373 (U4D).

The data can be read out to the 68000 through the logic provided. The 68000 sets up the address and sets the R/W\ line positive. It also indicates that it wants to address memory at line A23. The reception of these signals forces the 74LS197 counters (U2A and U4A) to follow the address from the 68000. When the signals AS\, UDS\ and LDS\ arrive, indicating that the address is OK and both of the data bytes are needed, the data is clocked out onto the data bus by 74LS244 (U2B) and 74LS125 (U4B).

4.5.10 Battery Current Measurement

A 759 power op-amp (U5L) is used for voltage supply, and is current limited by the 2.7 ohm resistor. When a voltage module is connected and a hearing aid is hooked up, current from the aid flows into the (-) input of the second 759 power op-amp (U4L). It is equipped with a 200 ohm feedback resistor, giving a 25 mA/5V conversion of current to voltage. Overdrive protection is provided by the catch diodes on the (+) input of the first op-amp and the use of the feedback catch transistor around the second op-amp. The output of the current converter circuit is connected to the proper input of the 4066 CMOS switch (U2J) through a 1 meg resistor so that it can be sampled when desired.

Bits 2 and 3 of input port (U2C) 74LS125 are also driven by switches on the battery box so that the battery substitution type can be read out.

4.6 High Speed Printer Board (061-0224-XX)

4.6.1 Printer Board

This printer drive board uses an eight bit 80C31 microprocessor to handle the decisions necessary to produce fast printing and feeding for the Fujitsu printer mechanism. The microprocessor also enables the board/printer to work with older versions of the 6500 and also with the older instrument, the 5500Z. RAM for the processor is formed by U19, PROM by U16. The processor clock is controlled by the 12 MHz crystal Y1. Since the processor shares address and data on the AD lines, the latch U12 is used to latch the AD lines during the first part of the printer CPU cycle to set the values of the A lines.

4.6.2 Printer Mechanism

The Fujitsu printer integrates the print head and circuitry for storage and burning the 320 dots on the head. It also has a thermistor that allows the detection of the temperature of the thermal print head for optimum control of the printing intensity. A four circuit stepper motor is used. The printer has paper out and head up detectors.

4.6.3 Motor Drive

Stepper motor drive is handled by use of a driver IC, U6. This chip automatically generates the stepping sequence when driven from pulses on its input pin 11 (from the printer CPU, port 1.6).

4.6.4 Burn Enable

The burn enable signals are provided by decoder IC, U10 (see 4.6.13, Fujitsu printer mechanism).

4.6.5 Burn Time Control

The length of the burn time is automatically controlled by the timer U1 and receives inputs from the available printer power supply voltage value, the thermistor in the printer, and the one shot drive signal.

4.6.6 Power on Reset

A power on reset circuit, U8, resets the circuits on the board on the startup of power. It is the same part that is used on the new HOST CPU. It also detects correct printer CPU operation by monitoring the ALE output from the printer CPU. The chip also

resets the printer CPU whenever the front panel RESET button is pressed. It does this through U3B, which is driven by the KB-RESET at pin 28 of J7.

4.6.7 Instrument Interface

Print commands and data from the 6500/C/CX (and 5500Z) are handled through U16 and U18. U18 is a simple eight bit latch, but U16 is a special four bit register with four locations. For the 6500, this data comes from the I/O board. The only path for data from the printer back to the 6500 CPU is the printer interrupt, INT-1.

4.6.8 Instrument Selection

The dip switch, S1, is used to program the printer board so that it can work with a particular instrument. When a 5500Z is used, a special interface board (Frye part no. 060-0225-XX) is plugged into J8. This board connects to the print pushbuttons of that instrument. The 5500Z also requires changing the resistors tied to the Data, IORD\ and IOWR\ lines from the bus connector, J7. A table is located on the upper right hand side of the printer schematic; this table tells the technician how to set the dip switch.

4.6.9 Logic Decoding

A PAL, U20, is used to decode logic. Pins 1 through 9 and 11 are used as inputs. Pins 13 through 19 are used as outputs.

4.6.10 Error Detectors

Detection of paper out is done by U3A and head up by U11C. It drives a beeper, DS1, through U5A and Q1. The beeper tells the operator that something is wrong. Circuits U4A and U4B inform the printer CPU of the problems. The beeping is controlled by P1.5 of the printer CPU through diode D2.

4.6.11 Miscellaneous Circuits

Several other flip flops are used for various tasks. The printer interrupt is handled by U17A. Slave65 FF, U17B, allows the printer CPU to communicate with the interface circuits U16 and U18. It also enables the feed and zero detect FFs to tell the printer CPU that they have been triggered.

A similar action by one shot FF U7A allows the printer CPU to operate the stepper motor driver. SMOE\ must be received from this one shot for the stepper motor driver to function. The printer CPU also knows that a printing operation is in process from the input on P3.2.

4.6.12 Power Supply

The power transformer is equipped with a winding that is used by the printer board. It comes in on J5. The power rectifier circuit produces an unregulated 24 volts DC.

4.6.13 Fujitsu Printer Mechanism

The Fujitsu printer mechanism can print 320 dots on one line. The data that is printed is shifted serially into a 320 bit shift register located on the print head. This serial data is presented to pin 7 of J2 from port 3.0/RXD of the printer CPU chip, and clocked in on the CLOCKIN signal at pin 9 from the inverting buffer U11F. U11F is driven by the printer CPU at the TXD output.

After all 320 bits are shifted, they are latched into a 320 bit burn register by P1.4 of the printer CPU. The 320 bits are burned 64 bits at a time. The burns are controlled by enable lines 1 through 5, getting steering indirectly from the printer CPU through U10.

This printer is also equipped with detectors for paper out and head up conditions and also contains a thermistor that is used to feed back the head temperature in order to optimize the burn time.

4.6.14 80C31 Microprocessor

The microprocessor is an 80C31, which contains on board RAM and is equipped with four ports The first port, port 0, acts as a dual address/data input/output port. Port 2 is used as an output port to provide upper order addresses to the printer board ROM and RAM. Port 1 is also an output port and supplies drive signals to many of the circuits on the board. Port 3 is multipurpose, and is used as a means of detecting the states of circuits and devices on the board, and also to drive several devices.

The processor also contains an internal oscillator circuit that uses Y1, a 12 MHz crystal, to control its frequency.

4.6.14.1 Address Latch

The printer CPU gets its instructions from the EPROM chip U14. It asks for instructions by address. The address comes from ports 0 and 2. The low order eight bits of the address from port 0 are presented on these lines only for a short period of time, and then the port is changed to a bidirectional data port.

The address data is made permanent by use of the latch U12 and the signal ALE from the printer CPU. This chip is driven by the ALE signal from the printer CPU to hold the low order address for devices which require it.

4.6.14.2 Chip Selects

Two signals are used for chip selects. PSEN\ and PSENRAM\ select PROM and RAM, respectively. PSEN\ comes directly from the printer CPU. PSENRAM\ is derived from signals at the input of the PAL, U20; these signals include PSEN\. The RAM chip can only be accessed when the Slave65 FF U17B is reset by a CLRSLAVE\ signal from the PAL.

4.6.14.3 Software Control

The printer CPU accesses the circuits on the board and also the digital data being sent from the host instrument bus. When print information is being received, Slave65 FF U17B is set, which allows the printer CPU to access the information in registers U16 and/or U18 which received the print information.

4.7 6500 Color Video Board (061-0121-XX)

4.7.1 General

This circuit board has been designed around the requirements of the VGA video monitor used for IBM and IBM Clone Personal computers. It uses a 82C450 video chip built by Chips and Technology.

The video circuit is also configured to only present this mode, and thus does not have the usual switching circuits employed in the usual VGA video board.

4.7.2 Oscillator

A single frequency of 50.35 MHz is used for both dot and memory clocks. The oscillator package is either an eight pin or 14 pin type with a CMOS output, and supplies power to CLK0 and CLK1 of the the 82C450.

The video chip has built in dividers to set the internal frequencies.

4.7.3 Video Chip Addressing

The first eight address lines of the 82C450 are time shared with an eight bit data bus. The remainder address lines are directly connected to the chip.

Address line 0 is created by use of the UDS\ strobe line from the CPU.

Address lines A1 through A13 are supplied by the address lines from the CPU.

Address lines A14 through A19 are supplied from an 8 bit port, bits 0 through 5.

The same addressing is used for both memory and I/O on the 82C450.

4.7.4 Control Port 100101

This port supplies two main functions. The first is that it controls whether the eight bit data sent to the 82C450 is a memory read or write or an I/O read or write. This is determined by the state of bit 7. A positive state on this bit signals a memory operation.

The second function of this port is the supplying of the last 6 address lines for the 82C450.

The port can be written to or read from, at the port address.

The 74ALS573 latch (U7) receives the write. The 74LS245 (U4) allows the port to be read.

4.7.5 Control Logic

The 16V8 PAL chip (U6) decodes the signals coming from the CPU and from the 82C450 and sends control signals to the different circuits. The following outputs are provided:

a. A20 read and A20 write signals to control the 8 bit control port discussed above in 4.8.4.

b. I/O read and I/O write signals for the 82C450 to tell it if the incoming data is valid for port (not memory) operations.

c. Memory read and write signals for the 82C450 for memory operations.

d. Upper data enable and lower data enable strobes to allow the interface of the 16 bit bus form the CPU to correctly interface with the eight bit 82C450 video chip.

These outputs are decoded form signals supplied from the CPU, the control port, and from the 82C450. The CPU signals include data to control reset operations and address strobes. The port supplies the bit that controls memory or I/O operations, and the 82C450 sends out information that signals whether address or data is being accessed.

4.7.6 Address/Data to the 82C450

Data is sent to and received from the chip through the 74LS245's (U5 and U8). The lower eight bits are handled by U5, and the upper eight by U8 on direction from the logic chip (U6). Direction is determined by the 82C450, but the video chip receives its information from a memory read or write command from the logic chip (6).

The lower eight bit address is handled through the 74LS541 (U3). It receives its instruction from the 82C450.

During a reset cycle, the 82C450 receives a byte of instruction from the resistors, R2 through R6. During reset, the address and data chips are disabled to allow these resistors to determine the instruction.

4.7.7 Dtack

The dtack circuit is formed by the 74LS01 (U1).

Dtack is immediately asserted upon receipt of a port read or write command by the connections from A20 read and A20 write drive lines. This means that the CPU performs a no wait state operation.

Dtack is controlled during 82C450 operations somewhat differently. Upper data enable and lower data enable signals immediately provide a dtack signal for no wait state operation unless the 82C450 demands a wait period be thrown in. If that occurs, the RDY line from the 82C450 is driven low which then holds off the dtack to the CPU. When RDY goes high, the Dtack is generated. RDY is normally in a high impedance state. RDY is apparently only asserted low during memory read operations.

4.7.8 Video Memory

Video memory is formed by the two 44C250 (U9 and U10) chips. The 82C450 chip has total control over the operation of these chips, and also provides refresh signals. The 33 ohm resistors are inserted into the circuit as damping elements.

4.7.9 Video Output

The video signal is composed of two parts, analog information for Z axis crt control and horizontal and vertical sync pulses. A third signal is sent to the video chip from pin 12 of the output connector. This line is driven low if a black and white, rather than color monitor is connected to the output.

The color analog signals are provided by the latch 74AC574 (U12) as latched through by the PCLK from the video chip. Signals from pins P0, P1 and P2 (blue, red

and green) are weighted with the resistor network (R14 through R22) so that they are twice as strong as those from P3, P4, and P5. The resistor matrix on the output is selected to provide a 0.75 volt peak video signal that is back terminated by an impedance of 75 ohms.

Blanking is generated by the video chip and is used to disable the output of the 74AC574 latch.

The color selection is made by the CPU program working in combination with the programming of the video chip.

Horizontal and vertical sync pulses are provided by the video chip and buffered by the 74F04 (U13) invertor.

The sense line is run directly to the video chip input. This line is normally set to +5 volts unless shorted to ground by a connection in the plugged in monitor. The zener diode D1 acts to protest the video chip from accidental electrical noise inputs that may damage the video chip.

4.8 6500-CX Probe Option

The 6500-CX probe option (Quik-Probe) includes the 6500 Interface Board (located inside the 6500-CX electronics module), the Quik-Probe remote module (hand held cable connected remote control) and accessories. The Quik-Probe remote module includes 4 circuit boards:

a. Keyboard
b. Preamp Board
c. Connector Board
d. EQ Board

4.8.1 Interface Board (061-0089-XX)

The 6500 Interface Board has the following functions:

a. Provides electrostatic discharge protection for the 6500-CX remote module connector. This protection is provided by keyboard inputs at J5 pins 2, 3, 4, 10, 11, 12 and 13; and by the audio input at J5 pin 8.

b. Provides power for the remote module; limits the available power to a non-destructive level in case of a shorted remote module cable. R23 and R24 limit the power available to the 7812 (+12 V) and 7912 (–12 V) 3 terminal regulators.

c. Interfaces between the 6500-CX and the remote module push button keys; latches rapid key strokes for later reading by the 6500-CX CPU. U3D and U1C form R-S flip flops. These flip flops are reset by the 6500-CX CPU after checking for a key stroke. Transparent latch U3B is permanently wired as transparent. It is used as a tri-state output buffer only. U3B couples the outputs of the R-S flip flops to the CPU data bus.

d. Switches the 6500-CX prescaler input between the M1550E sound chamber microphone and the remote module. (U2MB)

e. Controls the remote module REFERENCE MIC/PROBE MIC switch. (U2B)

f. Routes the signal from the Signal Generator Board to either the 6500-CX Power Supply Board audio power amplifier (to sound chamber) or else to the 6500-CX Interface Board audio power amplifier U3F (to Quik-Probe speaker).

g. Provides audio power amplifier for the Quik-Probe speaker. U3J is stable with gains greater than 10. Do not attempt to trouble shoot this circuit with gain less than 10. U3J has internal short circuit protection and internal over temperature protection. If the Quik-Probe speaker output is shorted, 6500-CX Power Supply Board resistors R16 an R18 may produce smoke and may open.

Note: The Quik-Probe SPEAKER LEVEL setting is dependent on the rear panel AUDIO SOURCE LEVEL setting.

4.8.1.1 Interface Board Connectors

J1	card edge	50 pins	Lower system bus
J2	card edge	50 pins	Upper system bus
J3	square pins	5 pins	to 6500-CX digitizer board
J4	square pins	5 pins	to 6500-CX rear panel, hand wired misc
J5	IC socket	14 pins	to 15 pin rear panel Remote Module Connector
J6	square pins	5 pins	to 6500-CX rear panel (M1550E) Microphone Input

4.8.1.2 Interface Board CPU Addresses

Note that D0 – D7 are the high, odd address byte; D8 – D15 are the low, even address byte. Away from the CPU board there is no address A0.

ADDRESS 100082H READ PORT (USE WORD READ not BYTE READ)

D0 D1 D2 D4 D5 D6	(Normally = 0) Each remote module key (except START/STOP) causes a unique combination of 2 bits to go to logic 1.
D3	Spare (logic 0)
D7	STOP/START; (normally logic 0) goes to logic 1 when START/STOP button is pressed or foot switch is pressed. Sense voltage = +18V to insure that foot switch contacts break through any oxide coating.
D8 – D15	Random; not used

ADDRESS 100080H WRITE PORT (USE WORD WRITE not BYTE WRITE)

D0	0 = sound chamber; 1 = Quik-Probe speaker
D1	0 = M1550E microphone; 1 = remote module selected microphone
D6	Remote module mic select; 0 = probe mic; 1 = ref mic
D7	Normally 1; set to 0 then back to 1 to reset the key sense R-S flip flops after reading the remote module keyboard
D2 D3 D4 D5	SPARE
D8 – D15	Not used

4.8.2 Keyboard (061-0086-XX)

There are only passive circuit elements on the keyboard. The keyboard connects the remote module to the 6500-CX cable to the preamp board. It contains etched switch contacts for use with silicon rubber switch buttons. Each switch, when pressed, will connect keyboard data lines to keyboard ground (or via 100 ohms to chassis).

Switch	**Keyboard**	**Interface Board**
Name	key pressed = logic 0	key pressed = logic 1
[<]	KD1 + KD6	U3B: D2 + D6
[>]	KD1 + KD4	U3B: D2 + D4
[\/]	KD1 + KD2	U3B: D2 + D1
[/\]	KD2 + KD3	U3B: D1 + D0
[MENU]	KD3 + KD4	U3B: D0 + D4
[DATA]	KD5 + KD6	U3B: D5 + D6
[LEVEL]	KD4 + KD5	U3B: D4 + D5
[STORE]	KD2 + KD6	U3B: D1 + D6
[PRINT]	KD2 + KD5	U3B: D1 + D5
[CLEAR]	KD3 + KD6	U3B: D0 + D6
[START/STOP]	KD7 (only)	U3B: D7 (only)
(foot switch)	KD7 (only)	U3B: D7 (only)
[SWEEP START]	KD1 + KD3	U3B: D2 + D0
[AIDED RESPONSE]	KD4 + KD6	U3B: D4 + D6
[UNAIDED RESPONSE]	KD3 + KD5	U3B: D0 + D5
[spare #1]	KD1 + KD5	U3B: D2 + D5 (not in use)
[spare #2]	KD2 + KD4	U3B: D1 + D4 (not in use)

The following connections are made between the remote module keyboard and the interface:

15 pin D connector pin	14 pin IC connector pin	Keyboard signal name	6500 Interface signal name
5	10	KD1	D2
12	4	KD2	D1
4	11	KD3	D0
11	3	KD4	D4
3	12	KD5	D5
10	2	KD6	D6
2	13	KD7	D7
			(START/STOP)
1	14	Mic Select	Mic Select
13	5	–12V	–12V
6	9	+12V	+12V
14	6	Headphone Gnd	Headphone Gnd
7	8	Audio	Audio
15	7	Mic Ground	Mic Ground
9	1	GND(K)	Keyboard Ground
(SHELL)	(BRAID)	KEYBOARD	SHIELD CHASSIS
8	(NC)	—	—

Notes: D0 – D7 are inverted from KD1 – KD7
D0 – D7 subscripts do not match KD1 – KD7 subscripts

4.8.3 Connector Board (061-0087-XX)

There are only passive circuit elements on the connector board:

a. The probe/reference microphone connector
b. The probe monitor headphones jack
c. The probe monitor headphones level control
d. The foot switch jack

4.8.4 Preamp Board (061-0088-XX)

This description is for preamp board 061-0088-04. Your preamp board should have suffix -04 or later for benefits of crosstalk improvements. If you have an -02 suffix, contact Frye Electronics for a replacement.

4.8.4.1 Ref Mic Preamp

U6 provides a high impedance load for the reference microphone and also a small amount of gain to allow calibration pot VR2 to be centered for the “average” reference microphone.

4.8.4.2 Probe Preamp

U2 provides a high impedance load for the probe microphone. Using the EQ board compensates for irregularities in probe microphone frequency response plus sensitivity, and rolls off high frequencies to avoid measurement error due to amplifier overload in later stages. (See Section 4.8.5 for a description of the EQ board.)

4.8.4.3 Mic Power

U4 provides a very low impedance power supply for the probe and reference microphones. Since the two microphones share this power supply, it must be regulated to prevent crosstalk between the two microphones.

4.8.4.4 Multiplexer

U3 simply switches the input of the line driver between the probe preamp and the reference preamp. U3A and U3B short the unused preamp signal to ground to further improve isolation between the two signals. U3 alternates between the two preamps at a rate of a few Hz as controlled by the 6500-CX CPU.

4.8.4.5 Mecca

In order to prevent interaction of the amplifiers on the preamp board, a single, very low impedance local ground reference is required. This ground reference is called “mecca” and is indicated on the schematic by a square with 9 circles inside. Mecca is tied to the remote module cable shield, a heavy braid, which is connected to 6500-CX chassis ground.

4.8.4.6 Line Driver

The line driver is also an “instrumentation amplifier”. The line driver translates the output signal “AUDIO” from mecca ground reference to 6500-CX microphone ground reference. The accuracy of match between 0.1% resistors R1/R2 and R4/R3 establishes the amount of rejection of ground noise between the 6500-CX and the preamp board. The line driver provides a low impedance output so that “AUDIO” will have no high frequency roll off due to cable capacitance. Note that the mic ground cable wire may have a few (less than 10) ohms of resistance.

4.8.4.7 Power Supplies

The remote module may be connected to the 6500-CX while the 6550-CX power is turned on. During this “hot plugging”, +12V, –12V, and ground may be connected in any order. CR1 and CR3 protect against reversed +12V and –12V supplies. CR2 and CR4 prevent +5V and –5V from interacting at power up. This interaction might prevent one of the +/–5 volt supplies from turning on. R21 and/or R23 will open during a gross fault.

4.8.4.8 Headphone Amplifier

The headphone amplifier allows the 6500-CX operator to listen to the output of the probe microphone. The headphone amplifier is intended to operate with 24–32 ohm Walkman style stereo headphones. U5, an NE5532 dual op amp, is specified to drive 600 ohm loads. Since R13 and R14 are 604 ohms each, the dual op amp will be unconditionally protected from output short circuits. The headphone amplifier will also work with monaural headphones. If the 6500-CX operator is hearing impaired, use 600 ohm headphones, which will provide louder output with this headphone amplifier circuit.

4.8.4.9 Microphones

The probe and reference microphones each contain a microphone element which in turn contains a FET source follower amplifier. Each microphone element has three terminals: +POWER, SIGNAL, and GROUND. Each micro-

phone element SIGNAL terminal receives current from a separate preamp board 47K resistor tied to –5V. This resistor is R8 for the probe mic and R25 for the reference mic.

4.8.5 EQ Board

The EQ board contains components to customize the probe microphone preamp gain and frequency response to match one individual probe microphone. (The serial number on the EQ board must match the probe microphone connected to the remote module.) The EQ board contains a high frequency boost circuit (pins 1, 2 and 3) and a low pass filter (pins 4, 5, 6 and 7) to remove frequencies above the 8000 Hz measurement limit of the 6500-CX.

5. CALIBRATION

There are few calibration adjustments on the 6500-CX, both external and internal to the instrument. Those available are covered in this section.

5.1 Microphone

The individual M1550 microphone is adjusted to the 6500-CX with the microphone calibration potentiometer located under the microphone input jack. A sound level calibrator, such as the Quest CA-12, with the adapter supplied, is used to supply a signal level at a calibrated intensity.

The microphone calibration potentiometer is located on the rear panel beneath the microphone input jack.

Turn noise reduction off.

When the calibrator is connected, the potentiometer is adjusted until the RMS reading agrees with the label on the calibrator.

5.2 Audio Source

The sound chamber drive amplifier gain is adjusted with the Source Output potentiometer. This matches the 6500-CX output level to that required by the speaker in the sound box.

Place the M1550 microphone in the sound box with the grill at the center of the reference point.

Switch off the 6500-CX and then switch it back on. Press RESET. Adjust the Source potentiometer until the RMS value of the sound level in the box is 70 dB SPL. This readout is at the right hand side of the real time display of the box spectrum.

5.3 Reference Mic Gain / Probe Mic Gain

Note: The PROBE microphone serial number must match the remote module EQ BOARD serial number. These are a matched set.

- Connect the Quik-Probe remote module to the rear of the 6500
- Turn 6500-CX power on
- Press 6500-CX [RESET]
- Press 6500-CX [PROBE]
- Press Quik-Probe remote module [MENU]
- Use Quik-Probe remote module [\/] key to select CALIBRATE PROBE
- Press Quik-Probe remote module [START/STOP].
- Install the Reference Microphone into a sound level calibrator. Adjust the remote module Reference Microphone gain pot. (to 110 dB for a Quest CA-12 Calibrator.)
- Install the Probe Microphone tube tip into the 1 mm to 14 mm adapter. Install the 14 mm adapter into the sound level calibrator. Adjust the remote module Probe Microphone gain pot. (to 110 dB for a Quest CA-12 Calibrator.)

5.4 Quik-Probe Speaker Level

Note: This adjustment is dependent on the 6500-CX rear panel AUDIO SOURCE LEVEL setting. Before attempting this adjustment, calibrate the probe and reference microphones per 5.3 above. This adjustment is not critical since the 6500-CX makes minor corrections for acoustics during the probe leveling process.

- Turn 6500-CX power on.
- Press 6500-CX [RESET].
- Press 6500-CX [PROBE].
- Press Remote Module [MENU],[\/],[>],[>], [MENU], [START]. This will put the 6500-CX into pure tone mode with a 1000 Hz tone present at the sound field speaker.
- Using the 044-0200-00 calibration clip, position the probe mic tube end at the center of the reference mic grill.
- Position the microphones 1 foot (30.5cm) away from the speaker directly in front of the speaker. There should be no objects or people within 2 feet (61 cm) of the sound field speaker or microphones.
- Press Remote Module [/\], [/\] to increase the SOURCE level to 80 dB SPL.

- Adjust the 6500-CX rear panel Quik-Probe SPEAKER LEVEL pot to 78 dB SPL as indicated by the 6500-CX MIC OUT display. When in actual use, there will be about 2 DB of increased microphone output due to reflections from the average patient's head.

6. MAINTENANCE

6.1 Line Fuse Replacement

If a fuse is blown for some reason, replace it with a like kind and voltage rating.

To change the fuse, first unplug the line cord from the voltage module. Then using a small screwdriver, pry the top of the module off at the notch near the line cord socket.

Replace the defective fuse located in the cover holder and replace the cover.

(See Section 8—Rear Panel Safety Markings.)

6.2 Line Voltage Module Change

The line voltage module is located at the rear of the instrument and is where the line power cord plugs in. It is possible to use several line voltages with this instrument. They are: 110V, 120V, 220V, and 240V. The voltages are marked on the module.

If the 6500-CX is going to be used in a country or locality where the line voltage will be different, the module must be changed to accommodate the voltage. The monitor must also be changed to one that is suitable.

To make a change, pry off the cover with a small bladed screwdriver placed in the slot next to where the line cord plugs into the module. Then again using the small screwdriver, pry out the small circuit board located in the end of the module. Note that there is a plastic device in the board that can be set to any one of four positions. The four positions correspond to the four voltages printed on the cover of the module. Rotate the plastic device until it is positioned as desired. Note that the arrow on the device must line up with a corresponding arrow in the body before the cover is replaced. The plastic tip will protrude through the cover of the module and point to the voltage selected.

If the voltages are 220 or 240, two small line fuses must be used. If the voltages are 110 or 120, a single line fuse of the 3AG size must be used. If the voltage must be changed from one size fuse to the other, then the small screw that holds the fuse holder in place on the cover must be loosened and the holder removed and turned over.

When the voltage and fuse have been set correctly, replace the module cover by snapping back into place.

6.3 Electronics Module

6.3.1 Removal and Replacement of the Wraparound

Removal
The electronics module can be serviced by first removing the wraparound. Remove the line cord and turn the module over on its back. It is a good idea to place the module on a smooth surface, and to cover the surface with a soft cloth to prevent scratching the cover and front casting. Remove the four screws at the extreme corners of the instrument. Place the module on its feet again. Remove the wrap-around by grasping at one edge on the side and flex it out and up. Do not try to remove it by sliding it off over the back. When you get the wraparound off you will see why sliding it off would be very difficult.

Replacement
When the time comes to replace the wraparound, use a slightly different procedure than was used for removal. There are retaining rubber strips built into the top underside of the wraparound that must be pushed straight down on the boards to properly retain them.

Place the wraparound so that the front edge is at the proper position on the casting and the rear panel. The front edge has the mounting screws closer to the edge than the rear.

Use both hands to spread the wraparound so that it slides straight down toward its final position. Once the slots for the support spacers have been cleared, it will slide down fairly easily. Keep pushing until it snaps into position on all sides, both front and rear. Replace the retaining screws.

6.3.2 Replacement of Plug-in Circuit Boards

The first step in replacement of a circuit board is the removal of the wraparound. See 6.3.1 for the correct procedure.

All circuit boards with active circuits are of the plug-in variety. They are easily replaced by unplugging connectors that go to them and then unplugging the board itself. Most of the boards are served with two main bus connectors, one on top and one on the bottom. The top connector must of course be removed first.

Note that when boards are replaced, that the small connectors that go to them are

color coded. Each connector has a specific color and a color dot marking one end, usually at pin number 1 of the connector. Be sure to match up the colors and the polarities of the connectors. The RS-232 cable connectors may be plugged in with the color dot up or down, depending on the desired communications mode.

6.3.3 Replacement of Main Panel

6.3.3.1 Front Casting Removal

Disconnect the line cord and remove the wraparound (see 6.3.1). Then remove the screws holding the front casting to the bottom metal chassis. Finally remove the 6 screws that hold the side and top support brackets to the front casting.

If it is necessary to completely remove the casting from the instrument, all of the connecting cables must be removed. Most repair procedures may be carried out by leaving the casting still connected to the main unit with some cables.

6.3.3.2 Removal of Front Panel and Circuit Board

The main front panel is disassembled from the front casting by unplugging the two cables and unscrewing the four nuts from the studs that hold the assembly to the casting.

Likewise, the front panel assembly is held together by four studs at the corners of the assembly. When separating the front panel and spacer from the circuit board, note that the rubber switches and plastic holders are retained in the front panel portion.

Reassembly of the board to the front panel should be done in reverse order, taking care that all rubber switches are properly located on their respective plastic frames.

6.3.4 Replacement of Power Switch

Remove the wraparound (see 6.3.1).

Locate the four wires connected to the rear of the power switch and make a note of how they are connected to the switch. Remove them by pulling them off straight toward the back panel. Also unplug the power indicator and the label indicator LEDs, noting the position and polarity of the plugs.

Locate the two 4-40 nuts at the top and bottom of the small panel where the power switch is mounted. Remove these nuts and lockwashers, and remove the small sub-panel on which the power switch and LEDs are mounted. The power switch is held

in by two expanding tabs, one on the top and one on the bottom. The switch is removed from the panel by squeezing the tabs and pulling the switch toward the front of the panel.

Installation of the switch is fairly simple — push the body of the switch into the hole until it can go no further. The expanding tabs hold it in place. Make sure that it is mounted right side up, with the red marker on the rocker pointed down.

Reposition the panel into the 6500-CX and, using the lockwashers, refasten it in place.

Replace the wires to the power switch and the connectors to the LEDs. Replace the wraparound (see 6.3.1).

6.3.5 Replacement of Printer Switchboard

Remove the wraparound (see 6.3.1).

This board is mounted to a switch. Removal and replacement of the entire assembly is necessary.

Remove the Printer Board and the front card guide to get better access to the switch. Unplug the LEDs and the ribbon connector. Note how they are positioned so that they can be replaced correctly.

Remove the screws holding the lower aluminum retaining bracket. Remove the upper screw holding the switch tab to the casting. Remove the switch assembly.

Replace in reverse order.

Replace the wraparound (see 6.3.1).

6.3.6 Replacement of Printer

Remove the wraparound (see 6.3.1).

Remove the cables that go to the printer from the connectors on the print board. Remove the four retaining screws that hold the printer to the bottom chassis. Remove the printer.

Replace with a new printer in reverse order.

7. CLEANING

For your safety, disconnect the 6500-CX from mains power while cleaning.

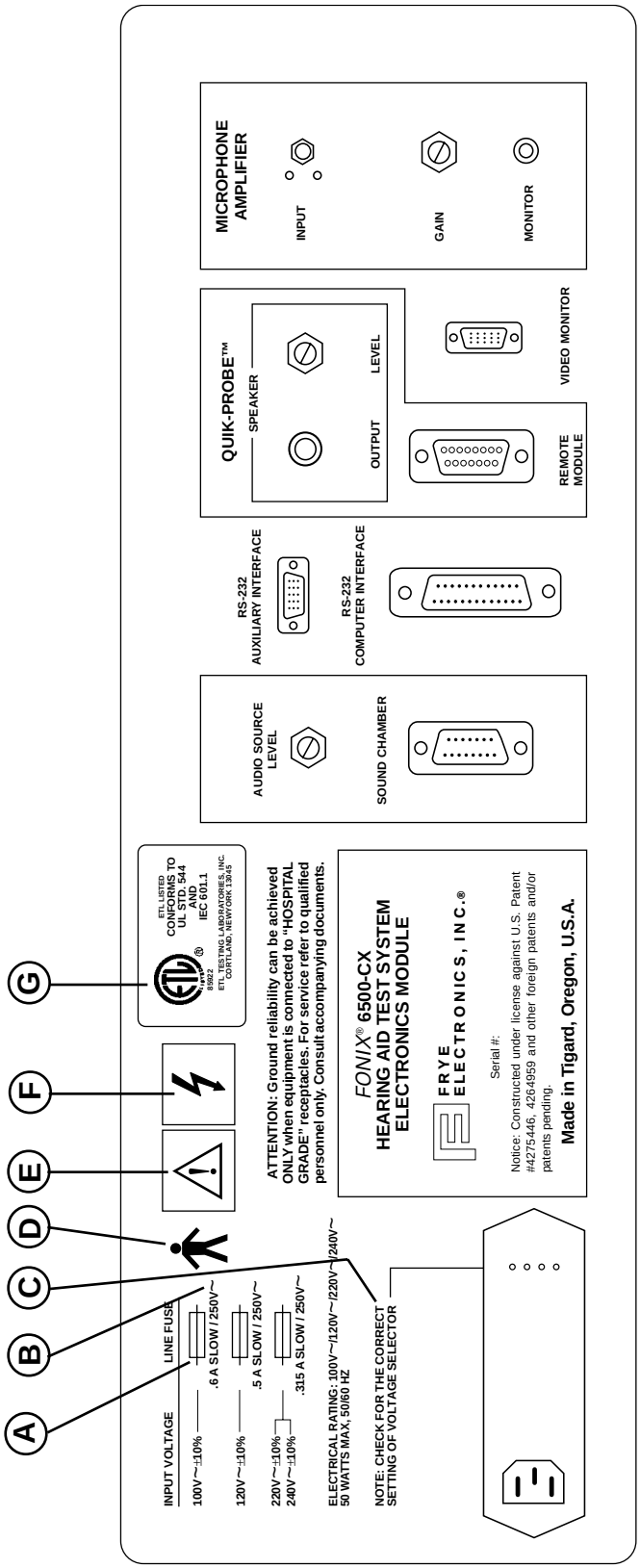
Wipe the 6500-CX with a slightly moist but not dripping cloth. Use plain water or water with mild dishwashing detergent. Wipe away any detergent with a slightly moist cloth, then dry the 6500-CX.

Never allow fluid to enter:

- the 6500-CX enclosure
- the 6500-CX power switch
- the 6500-CX voltage selector/power connector
- the 6500-CX electrical connectors
- the 6500-CX front panel push buttons

The microphones should be wiped with a dry cloth. Excess moisture may damage the microphone.

Solvents and abrasives will cause permanent damage to the 6500-CX.

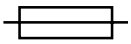


Rear Panel Layout

Letters identify rear panel safety markings

8. REAR PANEL SAFETY MARKINGS

Symbol **Meaning**

(A)  **"FOR CONTINUED PROTECTION AGAINST FIRE AND ELECTRICAL SHOCK, REPLACE ONLY WITH SAME TYPE AND RATING FUSE."**

For the 6500-CX, the mains fuse(s) depend on the mains voltage in your area.

Mains Input

Voltage	Qty	Type	Dimensions	Rating
100V	1	Slow (time delay)	1/4" x 1 1/4"	0.6A 250V
120V	1	Slow (time delay)	1/4" x 1 1/4"	0.5A 250V
220V	2	Time lag (type T)	5mm x 20mm	.315A 250V
240V	2	Time lag (type T)	5mm x 20mm	.315A 250V

Never replace a fuse with a fuse of rating higher than listed in the table above.

The fuse(s) must have at least one safety approval stamped on the fuse:

1/4" x 1 1/4" fuses: UL and/or CSA

5mm x 20mm fuses: Semco or British Electro Technical Committee (NCB, or other agency appropriate for your country.

5mm x 20mm fuses must conform to IEC 127 sheet III

(B) **250V ~** The " ~ " means AC, alternating current.

(C) **NOTE: CHECK FOR THE CORRECT SETTING OF VOLTAGE SELECTOR** (Please do this.)

(D) 

For purposes of safety classification under IEC60601-1, the 6500-CX is class 1 equipment, Type B.

"Type B" means the equipment is operated in the vicinity of a patient but there is no direct patient connection.

"Class 1 equipment" means that the 6500-CX chassis is connected directly to ground via the mains power cord. Safe operation of the 6500-CX absolutely depends on the integrity of the safety earth connection at your mains outlet. If you have any doubts concerning the adequacy of your mains outlet, contact a qualified electrician.

(E) 

"Read the accompanying documents "

(F) 

"Hazardous voltages inside. Refer service to qualified personnel."

(G) 

This symbol is provided on 6500-CX with safety approval option. A sample 6500-CX has been examined and tested by ETL Testing Laboratories. The 6500-CX conforms to :

IEC 601-1	Safety for countries outside the USA
IEC 801-2	Electrostatic discharge susceptibility
IEC 801-3	Radiated susceptibility
IEC 801-4	Conducted susceptibility
EN 50082-1	European community generic immunity
EN 55011	Group 1, Class A European community emission limits for industrial, medical, and scientific equipment.

ETL conducts routine site inspections of Frye Electronics.

Note that for the ETL listing to be valid, all mains connected electrical equipment attached to the 6500-CX must conform to IEC60601-1. Display monitors and computer equipment attached to the 6500-CX must be "medical grade" or else used with a medical grade isolation transformer.